

DESCRIPTION

Microsemi's LX1692B is a cost reduced, third generation CCFL (Cold Cathode Fluorescent Lamp) controller. The integrated controller is optimized to drive CCFL's using resonant full bridge inverter topology.

Resonant full bridge topology provides near sinusoidal waveforms over a wide supply voltage range in order to maximize the life of CCFL lamps, control EMI emissions, and maximize efficiency. This new architecture also provides a wide dimming range.

The LX1692B includes safety features that limit the transformer secondary voltage and protect against fault conditions which include open lamp, broken lamp, and short-circuit faults.

The LX1692B regulates the CCFL brightness in three ways: analog dimming, digital dimming, or combined analog and digital dimming methods simultaneously to achieve the widest dimming range (> 60 to 1).

The LX1692B can accept a brightness control signal that is either an analog voltage or a low frequency PWM.

The LX1692B also features integrated gate drivers for the four external power MOSFETs.

An integrated 4V LDO powers all internal control circuitry greatly simplifying supply voltage requirements.

The LX1692B is available in a 20-Pin TSSOP and SOIC.

IMPORTANT: For the most current data, consult MICROSEMI's website: <http://www.microsemi.com>
Protected by U.S. Patents: 5,615,093; 5,923,129; 5,930,121; 6,198,234; 7,112,929; Patents Pending

KEY FEATURES

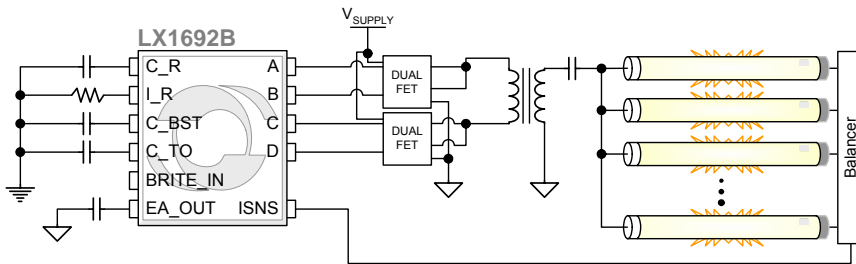
- For Wide Voltage Range Inverter Application (7V to 22V)
- Low Stress to Transformers
- Wide Dimming Range
 - Analog Dimming: >3 to 1
 - Digital Dimming: >20 to 1
 - Combined: >60 to 1
- Programmable Burst Dimming Frequency
- Programmable Time Out Protection
- Fixed Operating Frequency
- Open Lamp Voltage Protection, Short Lamp Protection, Arc Protection¹

BENEFITS

- Even Display Light Distribution
- Longer Lamp Life with Optimized Lamp Current Amplitude
- Reduced Operating Voltage Lowers Corona Discharge and Prolongs Module Life
- High "Nits / Watt" Efficiency Makes Less Heat and Brighter Displays

APPLICATIONS

- LCD TV
- LCD Monitor

PRODUCT HIGHLIGHT

PACKAGE ORDER INFO

T _A (°C)	PW	Plastic TSSOP 20-Pin	DW	Plastic SOIC 20-Pin
	-20 to +85		RoHS Compliant / Pb-free LX1692BIPW	

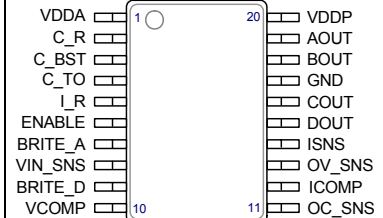
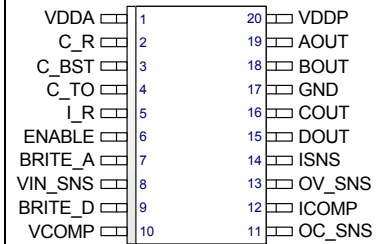
Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1692BIPW-TR)

¹ Arc protection is provided if the arcing level is enough to be triggered.

ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage (VDDP).....	6V
VIN_SNS	-0.3V to VDDP+0.5V
Digital Input (ENABLE).....	-0.3V to VDDP+0.5V
Analog Inputs (ISNS, OV_SNS, OC_SNS)clamped to ±14V Max Peak Current ±100mA	
Analog Inputs (BRITE_A, BRITE_D).....	-0.3V to VDDP +0.5V
Digital Outputs (AOUT, BOUT, COUT, DOUT).....	-0.3V to VDDP +0.5V
Analog Outputs (I_R, ICOMP, VCOMP).....	-0.3V to VDDP + 0.5V
Maximum Operating Junction Temperature	150°C
Storage Temperature Range.....	-65 to 150°C
Peak Package Solder Reflow Temp. (40 seconds maximum exposure).....	260°C(+0, -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

PACKAGE PIN OUT

PW PACKAGE
(Top View)

DW PACKAGE
(Top View)

RoHS / Pb-free 100% Matte Tin Lead Finish

THERMAL DATA
DW Plastic SOIC 20-Pin

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	85°C/W
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PW Plastic TSSOP 20-Pin

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	99°C/W
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Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.

The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

FUNCTIONAL PIN DESCRIPTION

Name	Description
C_R	Lamp Frequency Programming Capacitor Pin – lamp running frequency is set by the combination of C_R and I_R. The internal lamp current oscillator frequency can be forced to follow an external clock signal at this pin. In this case, the programmed frequency must be lower than the external frequency. Minimum pulse width for external synch signal is 1µsec. Maximum duty is 50%
I_R	Current Reference Resistor Input. Connects to an external resistor that determines the magnitude of the internal bias currents. The I_R pin is a DC reference voltage of 1V. This voltage should only be used for its intended function. The reference current established at this pin, by connecting an external resistor, is used to charge a capacitor at the C_R pin. The nominal lamp frequency can be adjusted by varying this resistor value in the range of 20K to 100K Ohms. (Note: C is in pF, R is in KΩ, Freq is in kHz). $F_{LAMP} = \frac{242 \times 10^3}{C_{C_R} \cdot R_{I_R}}$ Other reference currents derived from I_R are used for the digital dimming burst oscillator and the strike time out function.

FUNCTIONAL PIN DESCRIPTION (CONTINUED)

Name	Description
C_BST	<p>Burst dimming mode frequency set capacitor. Internal bias currents set via the I_R pin are scaled down and used to charge and discharge the capacitor connected at the C_BST pin. The voltage at the C_BST pin is a sawtooth waveform displaying a voltage that ranges from 0.5V to 2.5V. The frequency of the PWM for digital dimming is set by the I_R and C_BST pins.</p> $F_{DIM} = \frac{98039}{C_{C_BST} \cdot R_{I_R}}$ <p>where R_{I_R} is in KΩ and C_{C_BST} is in nF, F_{DIM} is Hz</p> <p>The internal burst oscillator frequency can also be forced to follow an external clock signal at this pin. In this case, the programmed frequency must be lower than the external frequency.</p>
C_TO	<p>Time Out set capacitor. An external capacitor is charged with an on chip current source to create a voltage ramp. Over voltage fault shutdown is disabled until C_TO voltage rises above 3.5V, providing a user programmed strike interval. Strike Interval time is $t = 0.035 R_{I_R} \cdot C_{C_TO}$ where R_{I_R} is in KΩ and C_{C_TO} is in μF</p>
VDDA	<p>Analog Voltage Regulator Output. This output pin is used to connect an external capacitor to stabilize and filter the on-chip LDO regulator. The input of the LDO is the switched VDDP supply. The LDO output is nominally 4.0V and is used to drive all circuitry except the output buffers at AOUT, BOUT, COUT and DOUT. The drop out voltage is typically 0.05V at 2mA; the average internal load. This output can supply up to a 5mA external load. The output capacitor should be a 100nF ceramic dielectric type.</p>
ENABLE	<p>Chip Enable Input. If logic high, all functions are enabled. If logic low, internal power is disconnected from the VDDP pin, disabling all functions. Logic threshold is 1.85V/1.35V maximum over supply and temperature range. Maximum current into VDDP when ENABLE < 0.8V, is 50μA. ENABLE may be connected directly to VDDP if the disable function is not used.</p>
BRITE_D	<p>Brightness Control Input for digital dimming. The input signal can be a DC voltage or low frequency PWM signal. Active DC voltage range is 0.5V to 2.5V. Signals above 2.5V makes continuous operation, voltages between 0.5V and 2.5V makes PWM digital dimming. Digital dimming pulse width varies from 100% duty at 2.5V to 0% duty at 0.5V. A minimum BRITE_D input voltage (externally supplied) of approximately TBDV is required to prevent fault stop. PWM inputs from either 3.3V or 5V logic are permissible. Frequency may range up to 1KHz. Max jitter of more than 1μs/V on this input may cause noticeable lamp flicker. Refer to Dimming configuration Table for setting.</p>
ICOMP	<p>Error Amp Output for the lamp current regulator. This error amplifier is a gm type and does not require an external capacitor for stability. An External capacitor is connected from this pin to Ground to adjust loop response of the inverter module. This capacitor value can vary from 0.1nF to 33nF as required by specific applications. Error amplifier output voltage is not allowed to exceed the peak voltage of its associated comparator ramp by more than 10%.</p>
VCOMP	<p>Voltage loop compensation pin for transformer output voltage regulation. An external capacitor is connected from this pin to Ground to adjust loop response. An external resistor divider can be connected to limit the maximum output duty cycle while the IC is operating in strike mode.</p>
BRITE_A	<p>Brightness control input for analog dimming. The input signal can be a DC voltage or a PWM signal that has been externally filtered to DC. Active DC voltage range is 0 to 2V. Signals above 2V and below 0.45V are clamped and do not change amplitude of output current.</p>
VIN_SNS	<p>Input voltage sense pin. An external resistor and capacitor are connected to this pin to control slope of the oscillator timing ramp. Ramp slope becomes steeper as the external bridge power supply increases providing rapid line voltage transient response.</p>

FUNCTIONAL PIN DESCRIPTION (CONTINUED)

Name	Description
OC_SNS	Over current sense input. The OC_SNS input is compared to a 2V reference. The comparator output shuts off the PWM outputs to prevent possible secondary failures. The input voltage at this pin is not rectified. Normal operating voltage levels will be in the range of $\pm 0.5V$ to VDDP. An abnormal voltage can operate continuously as high as $\pm 7V$ peak under load fault conditions. Transients under fault conditions up to $\pm 11 V_{PEAK}$ are permitted. An input voltage above 4 peak but less than $\pm 11V$ peak may cause saturation but will not cause malfunction, phase reversal, or reliability issues with the IC.
OV_SNS	Over Voltage Sense Input. This input pin monitors a voltage divider (approximately 1000:1) placed across the lamp. The open lamp voltage regulator uses it to regulate open circuit voltage. During both run and strike modes, fault detection comparators monitor voltage amplitude to determine if load opens occur. See functional description section for details on internal circuit operation. Frequency range of the input signal is from DC to 150KHz. Normal operating voltage levels will be in the range of ± 0.5 to $\pm VDDP$ peak, centered about $+0.2 V_{DC}$. An abnormal voltage can operate continuously as high as $\pm 7V$ peak under load fault conditions. Transients under load fault conditions up to $\pm 11V$ peak are permitted. An input voltage above $\pm 4V_{pk}$ may cause saturation, but will not cause malfunction, phase reversal, or reliability issues with the IC
ISNS	Current Sense Input. The ISNS input is full wave rectified by an On-Chip circuit, then presented to the inverting input of the current error amplifier. Frequency range of the input signal is DC to 200KHz. The ISNS pin also monitors lamp current to determine if the lamp is ignited. If a single cycle at the ISNS pin is greater than 1V, the strike / run flip flop is clocked to the RUN state and threshold of the strike comparator is lowered to 0.3V. During RUN mode current levels are continuously monitored to detect less than 0.3V. A counter clocked by RMPD_OUT is reset each time current is sensed at this input. If the counter overflows (256 counts) a fault latch is set which shuts down the IC. This fault is expected to occur when the lamp is shorted to ground through an impedance of less than 2K ohms or the ISNS resistor itself is shorted. The counter is inhibited during digital dimming off time. Normal operating voltage levels will be in the range of $\pm 0.5V$ to $\pm 5.5V$. An abnormal voltage can operate continuously as high as $\pm 7V$ peak under load fault conditions. Transients under fault conditions up to $\pm 11 VPK$ are permitted. Input voltages up 4V peak are linearly rectified. An input voltage above $\pm 4V$ peak but less than $\pm 11V$ peak may cause saturation but will not cause malfunction, phase reversal, or reliability issues with the IC.
DOUT	A buffer P-FET driver output. Has a 20K pull up, R_{DSON} nominal = 30Ω
COUT	A buffer P-FET driver output. Has a 20K pull up, R_{DSON} nominal = 30Ω
BOUT	A buffer N-FET driver output. Has a 20K pull down, R_{DSON} nominal = 30Ω
AOUT	A buffer N-FET driver output. Has a 20K pull down, R_{DSON} nominal = 30Ω
GND	Ground
VDDP	Input Supply Voltage, 4.5V to 5.5V input range. VDDP is switched (see ENABLE) to remove power from chip. An LDO regulator follows the switch and generates $4.0V_{DC}$. The output driver stages are powered directly from the VDDP input. The output capacitor should be a 1000nF or larger ceramic dielectric type.

ELECTRICAL CHARACTERISTICS

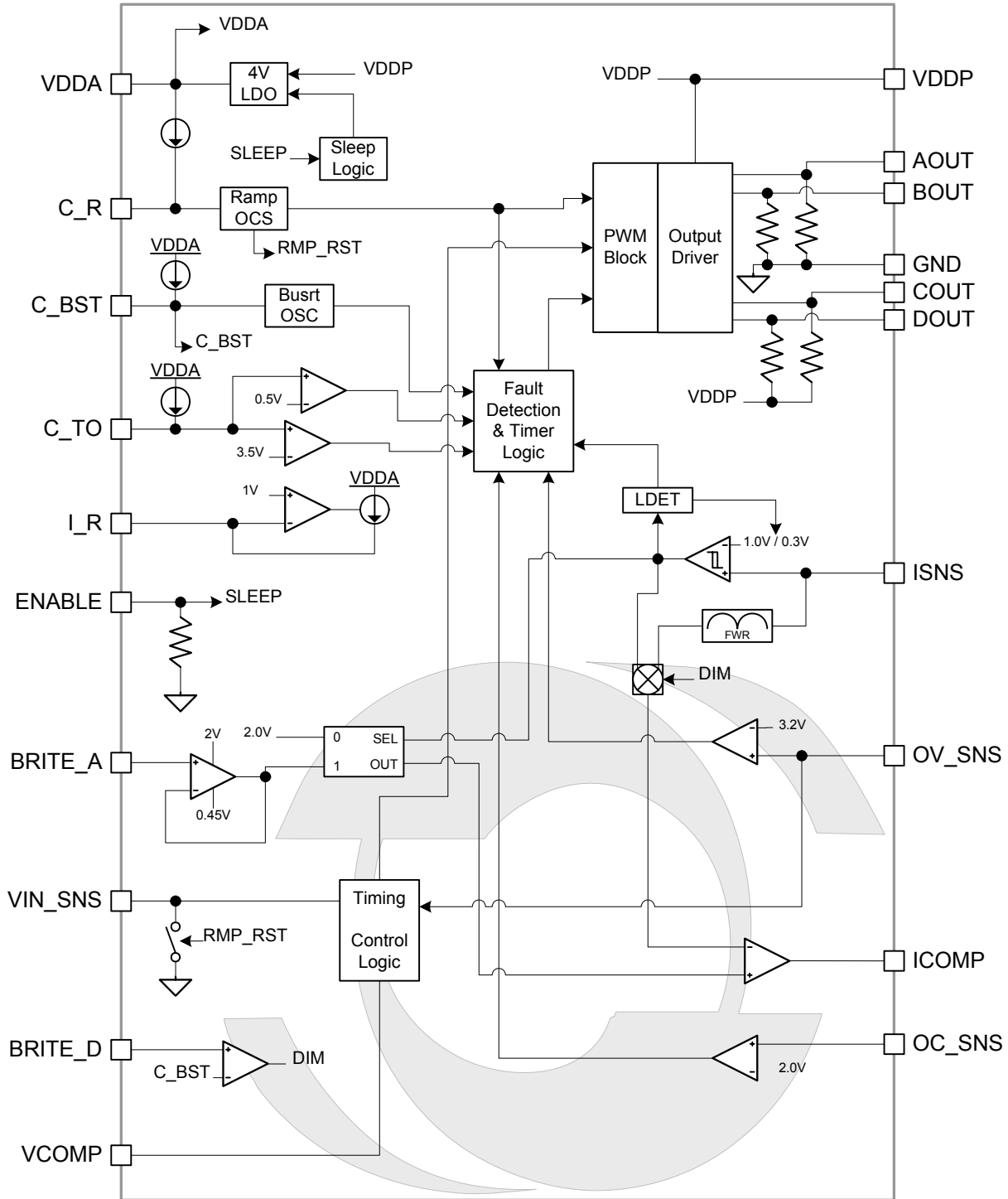
Unless otherwise specified, the following specifications apply over the operating ambient temperature $-20^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ except where otherwise noted and the following test conditions:

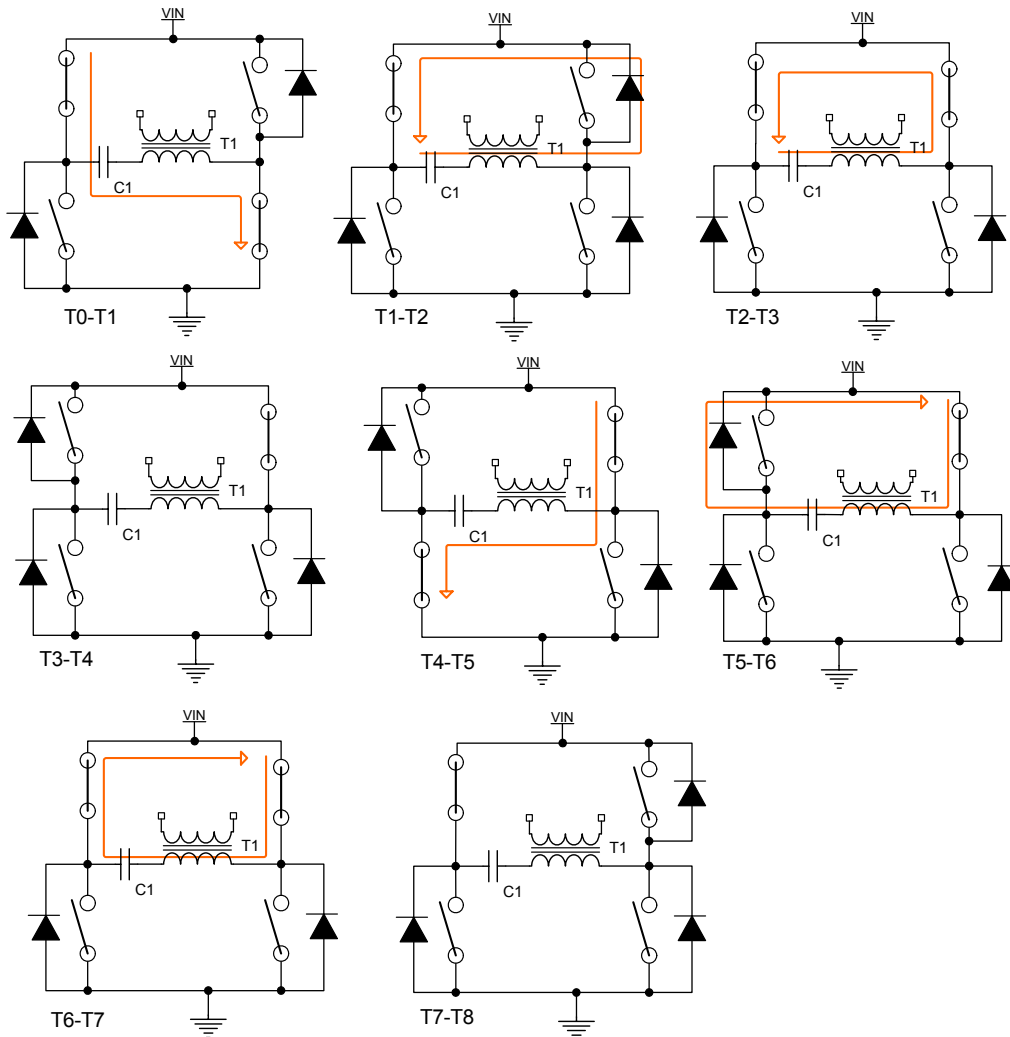
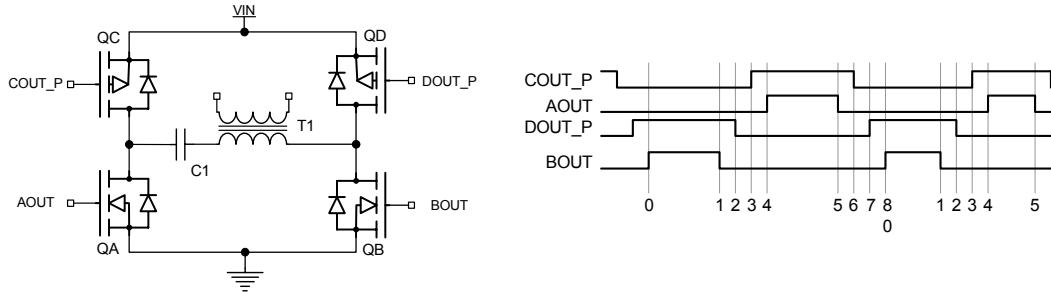
Parameter	Symbol	Test Conditions	LX1692B			Units
			Min	Typ	Max	
POWER						
Power Supply Input Voltage	VDDP		4.5		5.5	V
Power Supply Output Voltage	VDD_A	VDDP = 4.5V to 5.5V, I Load = 5 mADC	3.8	4.0	4.2	V
VDDP Operating Current	I _{SB}	f _{LAMP} = 62.5kHz, T _A = 25°C	3.8	5.3	6.8	mA
VDDP Operating Current	I _{BB}	C _{AOUT} = C _{BOUT} = C _{COUT} = C _{DOUT} = 2000pF, f _{LAMP} = 62.5kHz		10	15	mA
ENABLE INPUT						
ENABLE Logic Threshold	V _{TH_EN}		1.6	1.85	2.0	V
ENABLE threshold Hysteresis	V _{H_EN}			500		mV
ENABLE High	V _{EN_HIGH}		2.4		VDDP	V
ENABLE Low	V _{EN_LOW}		0		0.8	V
Sleep Mode Current	I _{DD_SLEEP}	V _{ENABLE} = 0V		20	50	μA
Input Resistance	R _{ENR}			100		KΩ
UNDER VOLTAGE LOCKOUT						
UVLO Threshold VDDP	V _{TH_UVLO_P}	Rising edge	3.8		4.2	V
UVLO Hysteresis	V _{H_UVLO}			200		mV
BRIGHTNESS CONTROL						
BRITE_A Voltage Range	V _{R_BR_A}		0		VDDP	V
Full Brightness BRITE_A Input	V _{BR_FULL_A}	V _{R_BR_D} = VDDA, T _A = 25°C	1.9	2	2.1	V
Full Darkness BRITE_A Input	V _{DARK_FULL_A}	V _{R_BR_D} = VDDA		0		V
Full Darkness BRITE_A input Offset	V _{DARKFULL_OS}	V _{R_BR_D} = VDDA, BRITE_A = 0V	0.35	0.45	0.55	V
BRITE_D Voltage Range	V _{R_BR_D}	V _{R_BR_A} = VDDA	0.4		VDDP	V
Full Brightness BRITE_D Input	V _{BR_FULL_D}	V _{R_BR_A} = VDDA, T _A = 25°C	2.37	2.5	2.63	V
Full Darkness BRITE_D Input	V _{DARK_FULL_D}	V _{R_BR_A} = VDDA	0.43	0.55	0.67	V
BURST RAMP GENERATOR						
Ramp Valley Voltage	V _{RVV}		0.43	0.55	0.67	V
Ramp Peak Voltage	V _{RPV}		2.37	2.5	2.63	V
Ramp Frequency	F _{RAMP}	C _{BST} = 10nF, I _R = 40K, T _A = 25°C	230	250	270	Hz
Burst Duty Cycle Range			0		100	%
BRITE_D to DIMPWM Jitter	J _{BDD}	C _{BST} = 10nF, BRITE_D = 2.4V		1	3	μs
Burst PWM min Duty Resolution	DR _{BST}				1	%
LAMP FREQUENCY GENERATOR						
Lamp Frequency Range	F _{LAMP}		30		150	kHz
Lamp Ramp Frequency	F _{LAMP}	Lamp Ignited, Run Mode, T _A = 25°C, I _R = 40K, C _R = 100pF	59.3	62.5	65.7	kHz
Lamp Ramp Frequency Regulation	F _{LAMP_REG}	4.5 ≥ VDDP ≤ 5.5V, T _A = 25°C VDDP = 5.5V			±0.5 ±0.1	% / V %/°C
Ramp Valley Voltage	V _{L_RVV}			0.2		V
Ramp Peak Voltage	V _{L_RPV}			2.0		V
Ramp PWM Jitter	LFJ				1	μs
VIN_SNS RAMP						
Ramp Peak Clamp Voltage	V _{RPCV}	V _{IN} = 8V, C _P = C _R = 100pF, R _P = 100K VDDP = 5V		5	VDDP +0.9	V
VIN_SNS Discharge Current	I _{VRV}		7	12.5	18	mA

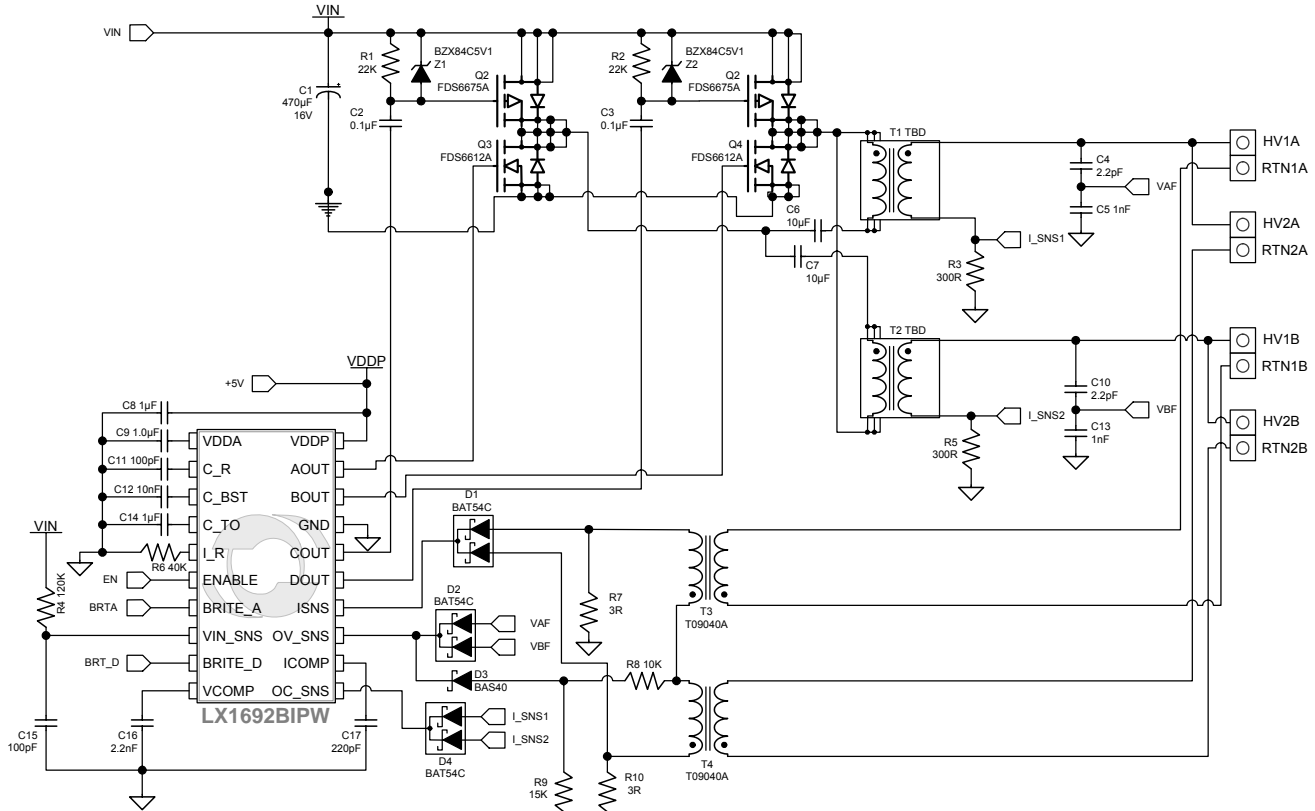
ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, the following specifications apply over the operating ambient temperature $-20^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ except where otherwise noted and the following test conditions:

Parameter	Symbol	Test Conditions	LX1692B			Units
			Min	Typ	Max	
BIAS BLOCK						
Voltage at Pin I _R	V _{IR}	I _R = 40K		1.0		V
Pin I _R Max Source Current	I _{MAX_IR}			75		μA
STRIKING BLOCK						
ISNS Input Strike Threshold	VISNS_STK		0.9	1.0	1.1	Vpk
Min ISNS Input Threshold	VISNSMIN		0.27	0.3	0.33	Vpk
Lamp current Regulation reference voltage during strike period	V _{REF_STK}		1.8	2	2.2	V
PROTECTION						
Open Lamp Detection Enable Threshold	V _{FEN}			3.5		V
Over Voltage Detection Threshold	V _{OVSTH}		3.0	3.2	3.4	V
Over Current Detection Threshold	V _{OCTH}		1.8	2.0	2.2	V
Open Lamp Striking Time Out	T _{STKO}	4.5V ≥ VDDP ≤ 5.5V, ISNS = 0V, C _{TO} = 1μF, I _R = 40K, VC _{TO} > 3.5V	1.2	1.4	1.6	sec
Open Lamp Time Out (After Ignition)	T _{OL}	VISNS < 0.3V, VC _{TO} > 3.5V, Lamp Freq = 60Khz		2.1		msec
Over Current Time Out	T _{OC}	VOC _{SNS} > 2.0V, Lamp Freq = 60Khz		500		μsec
Over Voltage Time Out	T _{OSL}	VOV _{SNS} > 2.9V, pulsed input		16		count
PWM BLOCK						
ISNS Input Voltage Range	V _{R_ISNS}	Maximum recommended for linear operation of error amplifier	-4		+4	Vpk
OC _{SNS} Input Voltage Range	V _{R_OC}		-4		+4.0	Vpk
OV _{SNS} Input Voltage Range	V _{R_OV}		-4		+4.0	Vpk
VIN _{SNS} Input Voltage Range	V _{R_VINS}		-0.3		VDDP	Vpk
ICOMP Error Amp Transconductance	G _{M_EAMP}	ISNS = 1.5V	100	220	410	μmho
ICOMP Output Source Current	I _{S_EAMP}	ΔV _{EAIN} = 1.0V		100		μA
ICOMP Output Sink Current	I _{SK_EAMP}	ΔV _{EAIN} = 1.0V		100		μA
ICOMP Output Voltage Range	V _{R_EAMP}		0		VDDA	V
ISNS-BRITE _A Input Offset Voltage	V _{OS_EAMP}	ISNS=1.5V, T _A =25°C	-100	0	100	mV
ICOMP Discharge Current	I _{D_ICOMP}			10		mA
ICOMP to A/B Output Propagation Delay	T _{D_COMP}			1100		ns
VCOMP High voltage	V _{HI_VCOMP}	VOVSNS = 0V,			VDDA	V
VCOMP Sink Current	I _{LO_VCOMP}	VVCOMP = 2V	1.5			mA
OUTPUT BUFFER BLOCK						
Output Resistance	R _{ON_SRC}	VDDP = 5V		30		Ω
Output Resistance	R _{ON_SINK}	VDDP = 5V		30		Ω
Pull Up Resistance	R _{UP}	COUT, DOUT		20		KΩ
Pull Down Resistance	R _{DN}	Aout, BOUT		20		KΩ
Output voltage High	VOH	C _{AOUT} = C _{BOUT} = C _{COUT} = C _{DOUT} = 2000pF	VDDP-0.4		VDDP	V
Output voltage low	VOL	C _{AOUT} = C _{BOUT} = C _{COUT} = C _{DOUT} = 2000pF	0		0.4	V
Min off time	t _{OFF}		200	320	550	ns

SIMPLIFIED BLOCK DIAGRAM

Figure 1 – Block Diagram

STATE DIAGRAM

Figure 2 – State Diagram

TYPICAL APPLICATION

Figure 3 – Schematic

FUNCTIONAL DESCRIPTION**OPERATING MODES**

Two operating modes, Strike and Run, are employed by the LX1692B. Upon power up or ENABLE going true, strike mode is entered. After a successful strike, e.g., lamp is ignited, run mode is entered. If ignition is unsuccessful, or if the lamp extinguishes while running, a fault is declared and the controller automatically shuts down.

OSCILLATOR CHARACTERISTICS

The main oscillator in the LX1692B has a fixed frequency loop. The fixed frequency loop is user set via the I_R resistor and the C_R capacitor value.

STRIKING THE LAMP

Lamp ignition is determined by monitoring the lamp current feedback voltage at the ISNS pin. If less than 1.0V during the strike period, the lamp is considered not ignited and Strike mode continues until ignition is detected or strike time out (approximately 1 - 2 seconds) is reached. If greater than 1.0V, strike is declared and a latch is set. The IC is now in "run" mode. And threshold voltage for strike detect is reduced to 0.3V to permit a minimum 3:1 analog dimming ratio to be achieved.

FAULT PROTECTION

The LX1692B has shut down protection for all common lamp fault conditions. These include the following:

- a. Open or broken lamp
- b. High Voltage Arcing on transformer secondary side
- c. Short from high side of lamp to ground
- d. Short from low side of lamp to ground (current sense resistor shorted)

Three inputs from the lamp are monitored to detect these conditions, ISNS, OV_SNS, and OC_SNS. Fault protection is designed to prevent fire or smoke from being generated by terminating inverter operation in the event of failures in the high voltage components and the power FET's. All fault shut down events can only be reset by ENABLE or VDDP cycling.

OPEN LAMP

When the IC is first powered on or enabled, the inverter output voltage must be made higher than the normal operating voltage of the lamp to cause ignition. The lamp may not ignite immediately when specified strike voltage is applied. It is customary to apply strike voltage for from 0.3 to 3 seconds to insure ignition of cold, dark, or aged lamps. The LX1692B has a programmable time out for this purpose. During strike time out, open lamp voltage is regulated to a value programmed by a voltage divider across the lamp and sensed at the OV_SNS pin.

Strike time out is programmed by selecting the capacitor value at the C_TO pin. If the lamp has not ignited before the end of strike time out, a fault is declared and the IC outputs are latched off.

HIGH VOLTAGE ARC OR OVER PROGRAMMED VOLTAGE

If a high voltage arc occurs due to intermittent lamp contacts or component failure, if the over voltage feedback divider is improperly designed, or if the open lamp voltage regulation circuitry fails, the peak voltage on the OV_SNS pin will rise above + 3.2 V_{DC}. This creates a pulse that increments a 4 bit accumulating counter. After 16 events are counted, an open lamp fault is declared and the IC outputs are latched off. This fault is enabled at all times, including during lamp striking. The 4 bit counter is reset by signal C_BST which typically operates at 100 to 300 Hz. Also, OVSNS pin voltage is greater than 3.2V, then ICOMP pin will be forced to discharge to 0V about 600ns.

OPEN LAMP VOLTAGE REGULATION

The open lamp voltage regulator regulates the peak voltage on the OV_SNS pin to +/- 1.97 volts, + the 0.2 volt offset, with a maximum tolerance +/-8% (+/- 158 mV). Assuming an additional +/- 5% tolerance for each of the two capacitors or resistors in the high voltage divider, maximum open lamp voltage tolerance at the system level is +/- 18%. At the high side of tolerance, OV_SNS peak voltage is +2.42V, on the low side of tolerance, OV_SNS input voltage will be regulated at +1.914 Vpk. If tighter total voltage regulation is needed in a given application, the feedback divider can be made with 1% resistors.

FUNCTIONAL DESCRIPTION (CONTINUED)
INTERMITTENT OR BROKEN LAMP AFTER SUCCESSFUL IGNITION

After run mode is entered, an intermittent or open lamp problem can also be detected at the ISNS input. After ignition, peak voltage on the ISNS input is dependent on lamp current amplitude and voltage on the BRITE_A pin. I_SNS signal amplitude should be designed to be greater than +/- 400 mV_{PK} (280 mV_{RMS}) to insure a false open lamp fault shut down does not occur. A comparator monitors ISNS and generates a reset pulse to a watch dog timer for any peak voltage > 0.3V. The watch dog, a 9 bit binary counter, is reset once every cycle of I_SNS voltage. If lamp current flowing through the ISNS resistor is too low (e.g., voltage is less than 0.3V peak), reset pulses are not generated and the counter is allowed to overflow and set the fault latch. Nominal short circuit duration is 500 micro seconds when operating at 65 KHz.

ON CHIP LDO REGULATOR

Output voltage is 4.0 +/-5%. Supplies all internal circuitry except output driver stage. Capable to source 5mA to external circuitry.

SHORT CIRCUITS ACROSS THE LAMP TERMINALS, SHORTS FROM THE HIGH VOLTAGE TERMINAL TO GROUND AND SHORT CIRCUITS FROM GROUND TO THE LOW SIDE LAMP TERMINAL.

A Short to ground from the lamp return terminal also shorts out the lamp current sense resistor, removing current feedback to the controller. This short is detected as a rise in voltage across the OC_SNS resistor which is located on the normally grounded side of the HV transformer secondary. A comparator senses peak voltage > 2.0Vdc at the OC_SNS pin. This comparator clocks the 4 bit watch dog timer described above in the open lamp fault logic. Sixteen events during a single cycle of the C_BST signal will overflow the watchdog counter and cause an over current shut down during either strike or run mode.

UNDER VOLTAGE LOCKOUT

Keeps chip outputs active off until VDDA is high enough to insure stable operation.

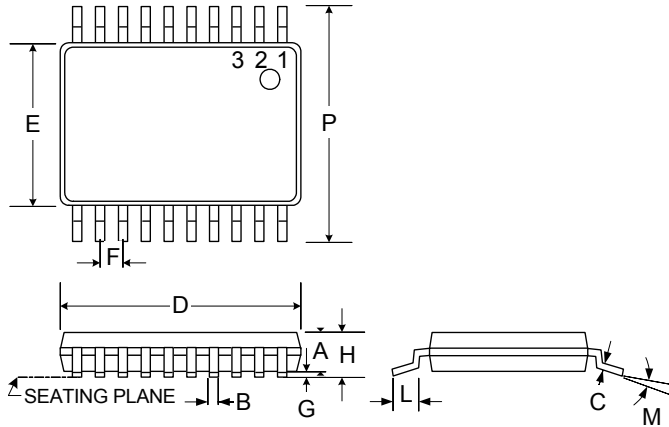
DIMMING MODES

Separate input pins are available for digital and analog dimming modes for maximum flexibility. See dimming truth table below. Digital dimming rise and fall times can be controlled by the ICOMP capacitor (See Dimming Modes Table).

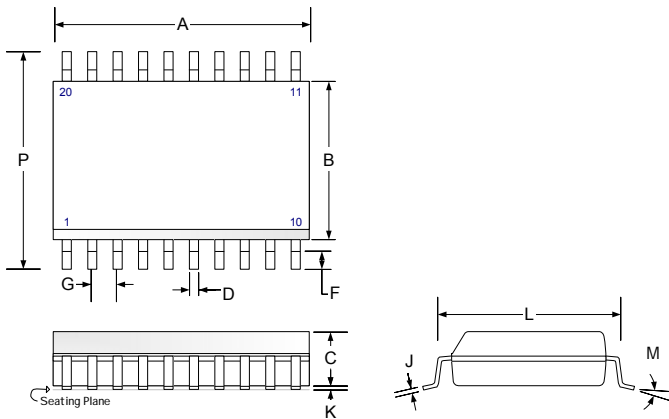
DIMMING MODES

MODE	BRITE A	BRITE D	ISNS	CBST	I Range
DC voltage controlled analog	0 – 2V	VDDA		cap	3:1
External PWM controlled digital	VDDA	PWM		cap	60:1
DC voltage controlled digital	VDDA	0.5-2.5V		Cap	30:1
Analog + voltage controlled Digital	0 -2V	0.5-2.5V		Cap	60:1

Note: For Reverse analog dimming, BRITE_A signal inversion must occur external to the controller

PACKAGE DIMENSIONS
PW 20-Pin Thin Small Shrink Outline (TSSOP)


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.10	-	0.043
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	6.40	6.60	0.252	0.260
E	6.25	6.55	0.246	0.258
E1	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
Θ1	0°	8°	0°	8°
*LC	-	0.10	-	0.004

DW 20-Pin Plastic (SOWB) Wide Body SOIC


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.85	0.498	0.506
B	7.49	7.75	0.295	0.305
C	2.35	2.65	0.093	0.104
D	0.25	0.46	0.010	0.018
F	0.64	0.89	0.025	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.10	0.30	0.004	0.012
L	8.13	8.64	0.320	0.340
M	0°	8°	0°	8°
P	10.26	10.65	0.404	0.419
*LC	-	0.10	-	0.004

*Lead Coplanarity

Note:

- Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.



Microsemi[®]

LX1692B

Full Bridge Resonant CCFL Controller

PRODUCTION DATA SHEET

NOTES

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