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Rev. B

Low Noise Chip Scale Atomic Clock
User's Guide

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REVISION SHEET for Document No. 098-00648-000

Revision	Reason for Change	Date	By
A	Initial release modified from 098-00055-000 (CSAC User Guide)	May 14, 2014	CDB
B	Revise Power Consumption per EC11030 from less than 250mW	November 16, 2015	SPD

Notices

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1 INTRODUCTION

The Microsemi Low Noise Chip Scale Atomic Clock (LN CSAC) combines the world's smallest, lowest power atomic clock technology with a high performance low power crystal oscillator to optimize both long term stability and phase noise peformance. The low power consumption of the LN CSAC, ≤ 290 mW, and exceptional phase noise performance, less than -120 dBc/Hz at 10 Hz offset, enables atomic timing accuracy in portable, battery-powered applications where higher performance phase noise is necessary.

This manual describes the use of the **CSACdemo** software along with the LN CSAC **Developer's Kit** (Part # 990-00565-000), which includes an evaluation board, cabling, and power adapter. Installation and use of the **Developer's Kit** is presented in **Section 3.4** of this User's Guide. The descriptions of LN CSAC functionality in **Section 4** include examples from the **Developer's Kit**. **Section 5** contains detailed programming information for systems' integrators.

2 REFERENCE DOCUMENTS AND TECHNICAL SUPPORT

Supporting information specific to LN CSAC is available from http://www.microsemi.com/lncsac. This includes the LN CSAC datasheet, **CSACdemo** install software, Gerber files, schematic, and the bill of material for the evaluation board used in the Developer Kit, in order to facilitate mechanical, electrical, and functional integration of the LN CSAC into users' systems and applications. Please contact Microsemi's Applications Support group at the contact info below for further assistance or support for non-standard applications. For additional documentation, please contact your Microsemi sales representative or visit us online at www.microsemi.com.

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3 LN CSAC OVERVIEW

3.1 PRECAUTIONS

Caution: To avoid electrostatic discharge (ESD) damage, proper ESD handling procedures must be observed in unpacking, assembling, and testing the LN CSAC.

The LN CSAC is delivered in ESD-safe packaging. The LN CSAC should only be removed from the ESD-protective bag in an ESD-safe environment. Once installed on the test fixture, the ESD sensitivity is considerably reduced. However, it is recommended that the entire assembly be treated as ESD-sensitive insofar as possible.

3.2 PACKAGING

Please retain the original LN CSAC ESD-safe packaging material in the event that the device needs to be returned to Microsemi for service.

3.3 ABSOLUTE MAX RATINGS, LN CSAC MECHANICAL AND SPECIFICATIONS

Please refer to the product datasheet for all specifications and handling requirements specific to the LN CSAC product. The product datasheet is available from the download location listed in Section 2.

3.4 DEVELOPER'S KIT

The LN CSAC Developer's Kit includes all of the necessary hardware, software, and cabling to facilitate validation of performance, brass-board demonstrations, and software interface development.

3.5 PACKAGE CONTENTS:

The Developer's Kit (Part # 990-00565-000) includes:

Item	Microsemi Part Number	Notes
Evaluation Board	089-00794-000	
Power Adapter	140-00041-000	5 VDC 5mm center positive
RS232 Cable	060-00322-000	
Introduction Doc	689-02461-000	

Table 1: Contents of the LN CSAC Developer's Kit (part # 990-00565-000)

Please contact Microsemi if any of these items are missing.

3.6 INSTALLING THE LN CSAC ON THE TEST FIXTURE

Caution: To avoid electrostatic discharge (ESD) damage, proper ESD handling procedures must be observed in unpacking, assembling, and testing the LN CSAC Prototype.

Remove the LN CSAC and evaluation board from their ESD protective bags only in an ESD-safe environment. Note that the LN CSAC's pinout is "keyed" so the LN CSAC can only be inserted in the proper orientation. Before any power is applied to the board, carefully ensure all pins are correctly seated in their sockets and gently insert the LN CSAC into the socket on the evaluation board as shown in **Figure 1** below.

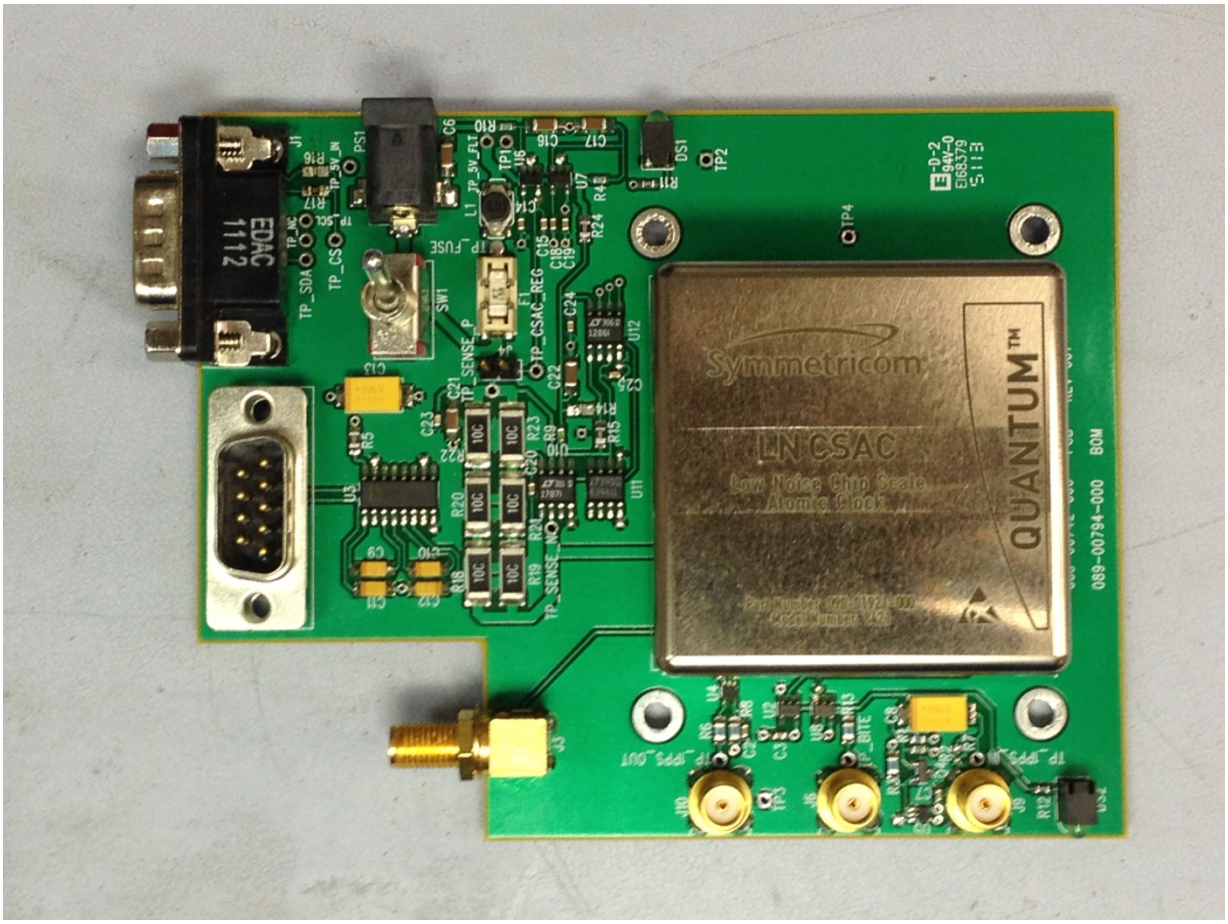

Figure 1: LN CSAC on evaluation board

3.7 INSTALLING THE CSACDEMO SOFTWARE

The Microsemi **CSACdemo** software (Part # 084-00365-000), available from the download location listed in Section 2, provides a convenient graphical user interface for monitoring and controlling the LN CSAC as well as other products from Microsemi's LN CSAC family. **CSACdemo** also is used for collecting and archiving monitor data from the LN CSAC. It will install and run on any PC running Microsoft Windows® XP or Windows® 7 and having at least one available RS232 (COM) port. Note that multiple LN CSACs can be monitored from a single PC, provided additional COM ports are available.

To install the **CSACdemo** software, double-click on the downloaded file or click on **Run…** on the Windows **Start** menu and type **"*x*:\setup.exe**" where "***x***" is the drive letter and directory where the setup file was downloaded.

Upon accepting all of the default installation options (recommended), the **CSACdemo** software will be installed in **c:\Program Files\Microsemi\LN CSAC**, a startup icon will be added to the **Start→All Programs→Microsemi→LN CSAC** menu, and a **CSACdemo** icon will be placed on the desktop.

3.8 CABLING

Connect the provided RS-232 cable between the evaluation board and the COM port on the PC. On laptops without an available COM port, a USB-to-RS232 adapter such as National Instruments USB-232 can be used. We have tested many of these. Most of them work, some do not.

Make sure the power switch on the evaluation board is in the off position as shown in **Figure 2**. Connect the 5V power adapter between the 5V power input and a 120 VAC wall outlet.

LN CSAC signal outputs are available from the evaluation board on connectors **J3** (10 MHz Out) and **J10** (1 PPS). Connect either (or both) of these to your test equipment (frequency counter, spectrum analyzer, etc.)

3.9 EVALUATION BOARD OVERVIEW

Detailed schematics of the evaluation board are available from the download location listed in Section 2. **Figure 2**, below, shows the primary features of the evaluation board.

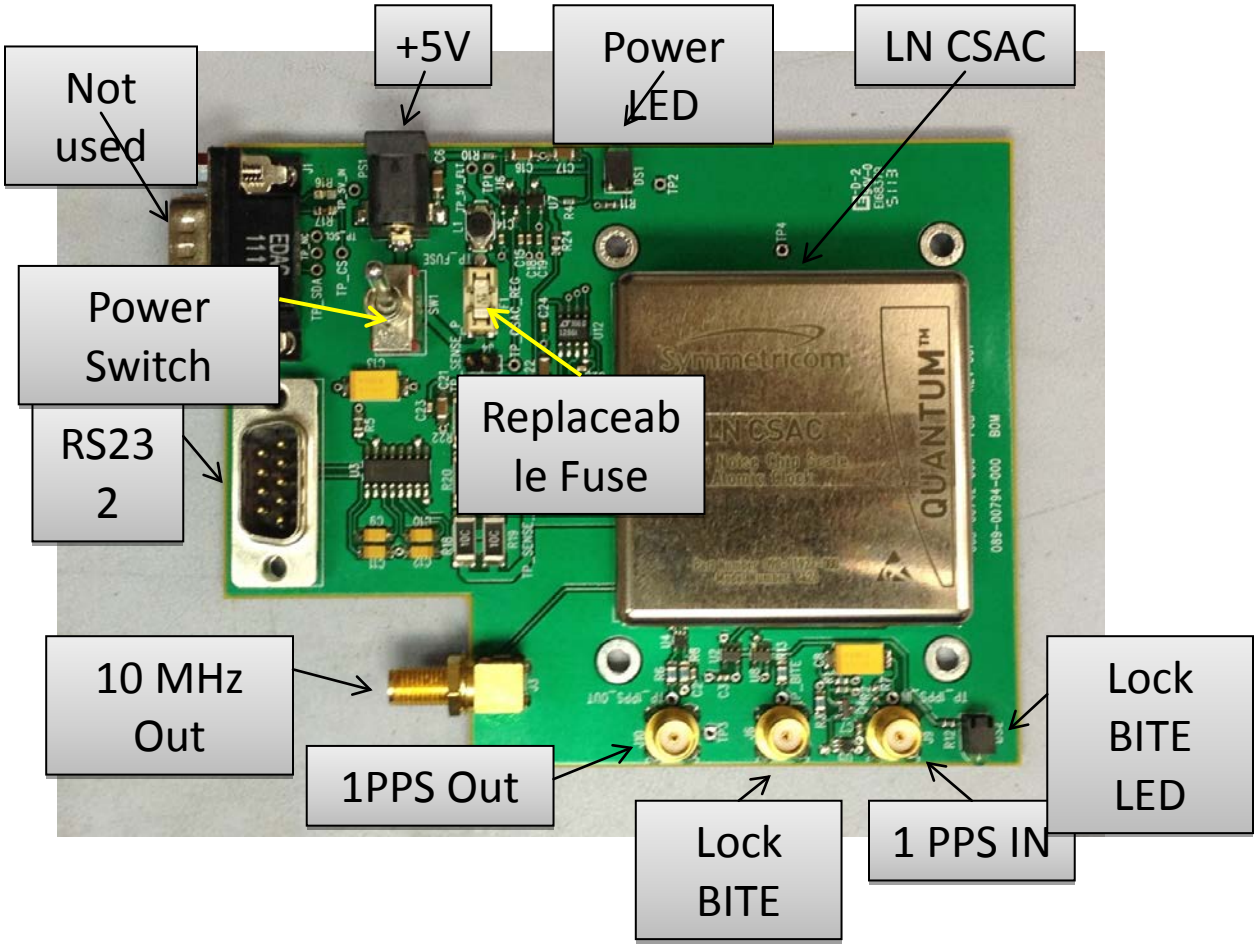

Figure 2: Test Fixture Connections

10 MHz Out (**SMA**) – The LN CSAC output is a sine wave output capable of delivering up to 9 dBm into a 50 ohm load.

Replaceable Fuse – Replacement fuse: Littelfuse Part No. 0453 01.5

5 VDC Input – Input power to the evaluation board is provided on a 5 mm (center positive) coaxial connector (PS1). To avoid damage to the test fixture, it is highly recommended to use only the power adapter which provided by Microsemi with the **Developer's Kit**, and to not insert or remove the LN CSAC while power is applied.

RS232 Connection (DB9M) –The evaluation board provides a level shifter (U3), which converts the LN CSAC 0-3.3 VDC serial interface to the RS232 standard +/- 12 V for direct interface with a PC COM port. Connect the test fixture (J2) to a PC with the standard (non-Null) DB9F-DB9F RS232 cable, as provided by Microsemi with the **Developer's Kit**.

Lock BITE LED – Indicates normal operation following initial acquisition of the clock signal. Note that this is the logical complement of the BITE output (LN LN CSAC PIN 4).

Lock BITE (SMA) – This is a buffered output from PIN 4 of the LN LN CSAC.

Power Switch – Controls power to the evaluation board and to the LN LN CSAC.

Power LED – Indicates the state of the **Power Switch**.

1 PPS Input (**SMA**) – The 1 PPS input connection to the evaluation board accepts a 1 PPS reference of arbitrary amplitude (logic high: $2V < V_{in} < 20V$) and generates a 0-3.3 V CMOS pulse to the LN CSAC. Note that this input is capacitively coupled to the level-shifting circuit on the evaluation board (see schematic available from the download location listed in Section 2) and therefore the applied pulse width must be < 10 ms in duration.

1 PPS Output (**SMA**) –The 1 PPS output is buffered by a CMOS 0-3.3 V logic gate on the evaluation board.

3.10 INITIAL START UP

3.10.1 Initial Power-On

Connect power and RS232 to the Evaluation Board as described in Section 3.8, above.

Turn on the power switch on the Evaluation Board.

Double-click the **CSACdemo** icon on the connected PC.

3.10.2 Establishing Communications

When communications are successfully established, the **CSACdemo** main window appears as shown in **Figure 3**.

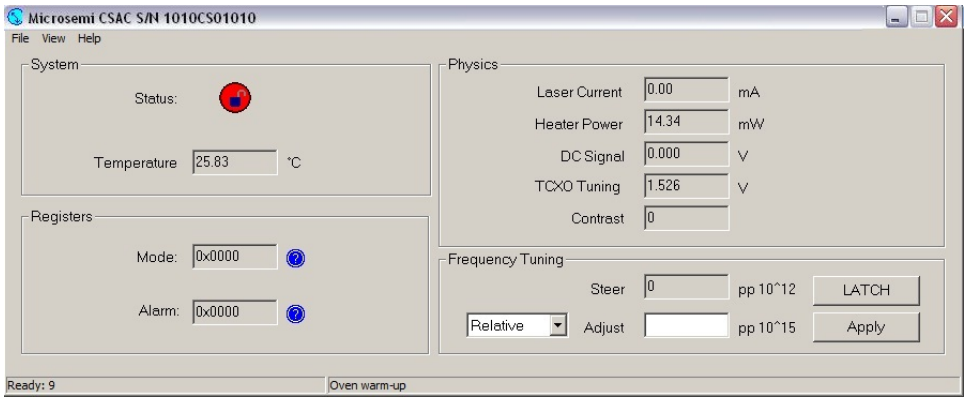

Figure 3: CSACdemo communicating with LN CSAC during warm-up

The title bar of the window indicates the Unit Serial Number (here "1010CS01010"). The main body of the window shows most of telemetry values from the unit (see **5.4.1** for telemetry descriptions). Initially, upon power-up, the status indicator ("") reflects the LN CSAC's unlocked condition (**BITE**=1). The left field of the bottom status bar indicates the number of seconds until the next poll (here "9") and the right field indicates the unit status (here "Oven Warm-up").

In the event of communication failure, the Status indicator appears as "". In this case, check the cabling, power supply, etc. The bottom left status bar may also indicate the source of the communication failure. If the COM port is in use by another application, the status bar will report "RS232 open failed," otherwise, it will likely indicate "Instrument not responding". If you are using a PC serial port other than "COM1," you may need to select **Options…** from the **File…** menu and select a different **Com Port** as shown below in **Figure 4**. Select the correct

COM port from the pull-down menu and click on **"Apply Changes"** to re-attempt communications. Note that just pressing "**OK**" with not pressing "**Apply Changes**" will not accept any changes that have been made.

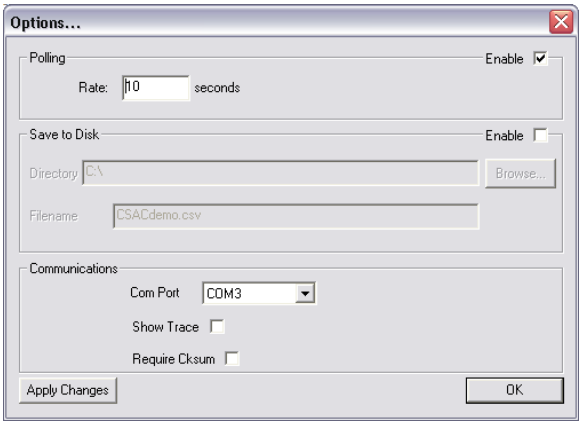

Figure 4: CSACdemo Options... panel

Once the cable connections have been checked and the **COM Port** is set correctly, you should be able to achieve communications similar to the appearance of **Figure 3**.

3.10.3 Monitoring Communications

For development of application-specific embedded firmware for LN CSAC, it is helpful to observe the communications between the **CSACdemo** program and the LN CSAC. Enable the **Show Trace** checkbox in the **Communications** section of the **File - Options…** panel and remember press **Apply Changes** prior to pressing **OK** to view the bi-directional protocol.

With the trace visible, the **CSACdemo** main panel appears like:

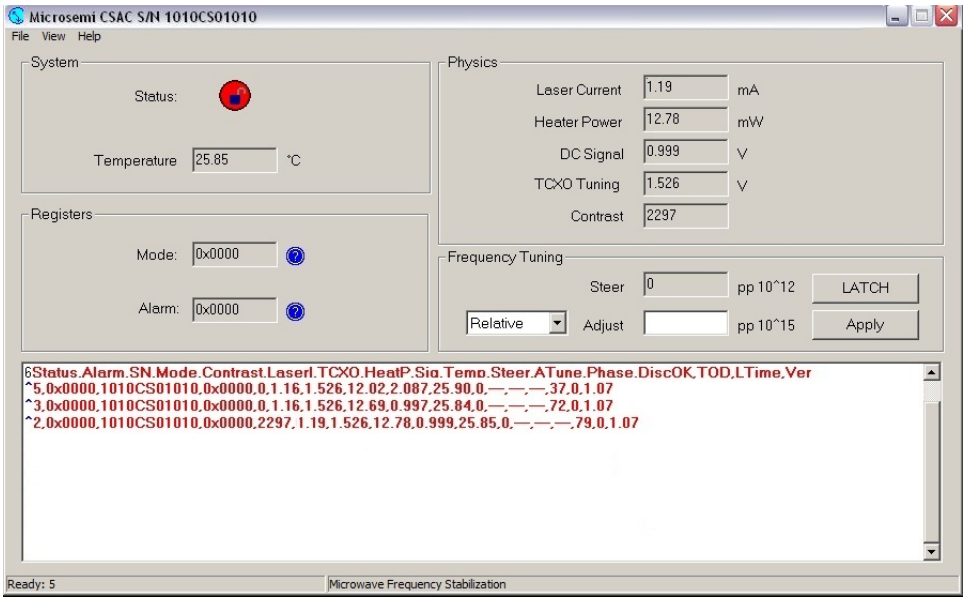

Figure 5: CSACdemo main panel with communications trace visible

Note that communications from the host PC to the LN CSAC are shown in BLUE and communications from the LN CSAC to the host are shown in RED.

3.10.4 Observing Acquisition

Initially, when the LN CSAC is powered up, the lock LED on the evaluation board will momentarily turn on then off once again. During acquisition the **Unit Status** field in the lower right corner of **CSACdemo** will proceed through the stages corresponding to the values of the **Status** register (see **Error! Reference source not found.**).

Acquisition takes < 2 minutes in a 25°C ambient (up to a maximum of 5 minutes at -40°C). When acquisition is complete, the lock LED on the evaluation board will illuminate, the **CSACdemo** right hand status bar will indicate "Locked," and the status indicator will change from " " to " ".

Once locked, the main panel of **CSACdemo** appears similar to **Figure 6**.

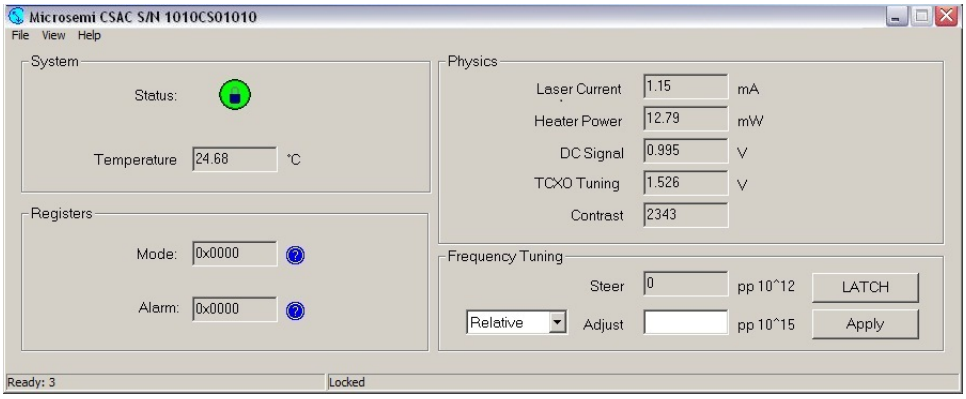

Figure 6: CSACdemo in locked condition

Figure 6 shows typical values for a normally operating LN CSAC. In this case, the internal case temperature of the LN CSAC is 24.86°C, the operating mode is 0x0000 (see **5.4.3**) and there are no alarms. The physics package parameters in **Figure 6** are fairly typical as well: The laser current is about 1.15 mA, the physics package heaters are drawing less than 25 mW, and the DC signal level is about 1 V. The OCXO tuning is mid-range on 0-2.5V and the contrast is comfortably above 1000.

3.11 DATA ACQUISITION WITH CSACDEMO

For long-term monitoring of the LN CSAC, select the **Options…** panel from the **File** menu (see **Figure 4**).

Choose a polling rate in seconds. For short-term (1-2 day) measurements, a polling rate of 10 seconds is optimal, and will accumulate data onto disk at a rate of about 1 MB/day. For longer term measurements (30-100 days), a longer polling rate, such as 60 seconds, will reduce the growth of the data file to 150 KB/day. In any case, the files are relatively small by modern standards.

Enable **Save to Disk** with the checkbox in the top right of the panel.

Use the **Browse…** button to select an existing **Directory** in which to archive the LN CSAC data. Note that you must have write permission to the selected directory. Type in a **Filename** for the Data.

When you are finished, the panel might look something like:

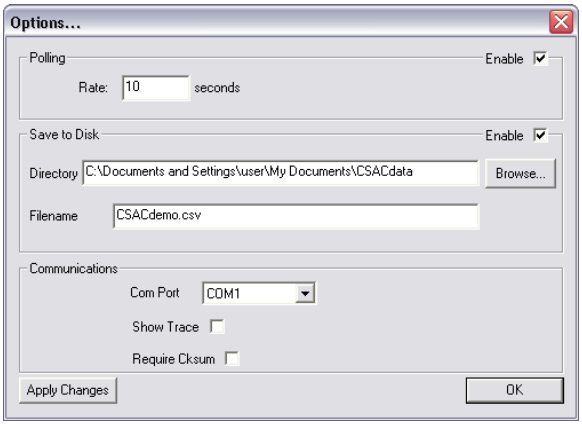

Figure 7: CSACdemo options for datalogging to disk

Click **Apply Changes** to implement the new options or **OK** to discard changes and exit the panel.

The data is stored in ascii comma-separated-values (CSV) format, which allows for convenient import into most popular spreadsheet and analysis software. The first line in the file contains the column headers (see **5.4.1**, "**!6**" command). Subsequent lines contain the corresponding periodically-polled data (see **5.4.1**, "**!^**" command). The first column in the file contains time stamps, derived from the host computer's clock, in mean-Julian day (MJD) format, referenced to universal coordinated time (UTC).

4 FUNCTIONAL DESCRIPTION

4.1 PRINCIPLE OF OPERATION

The LN CSAC is a passive atomic clock, incorporating the interrogation technique of Coherent Population Trapping (CPT) and operating on the D1 optical resonance of atomic cesium. A complete description of passive atomic clocks, CPT, and the LN CSAC architecture is beyond the scope of this **Users' Guide**. The following description should be adequate for users and systems integrators.

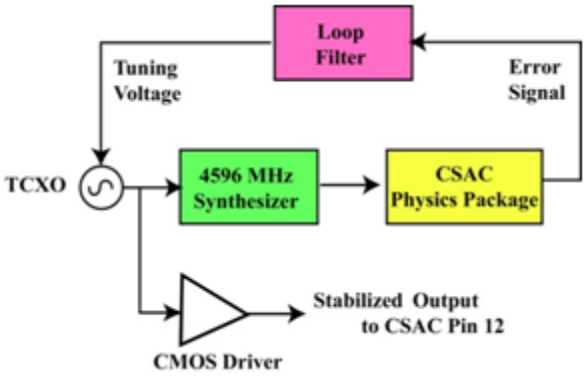

Figure 8: Simplified LN CSAC block diagram

Figure 8 shows a simplified block diagram of the LN CSAC, omitting the AC coupling and passive filtering after the CMOS driver. The principal 10 MHz output from the LN CSAC is provided by a temperature-compensated crystal oscillator ("OCXO") which is buffered by a CMOS logic gate and provided after AC coupling and filtering on the LN CSAC output pin 3. In normal operation the frequency of the OCXO is continuously compared and corrected to ground state hyperfine frequency of the cesium atoms, contained in the "physics package," which thereby improves the stability and environmental sensitivity of the OCXO by 4-5 orders of magnitude. In addition to the OCXO and the physics package, which is described in detail in [1], the essential components of the LN CSAC are the microwave synthesizer and the microprocessor (see [2]). The microwave synthesizer generates 4596.3*x* MHz with microprocessor-controlled tuning resolution of approximately 1 part in 10^{12}. The microprocessor serves multiple functions, including implementation of the frequency-lock loop filter for the OCXO, optimization of physics package operation, state-of-health monitoring, and command and control via RS232.

When the LN CSAC is initially powered on, it performs an acquisition sequence which includes stabilizing the temperature of the physics package, optimizing physics package operating parameters, and acquiring frequency lock to the atomic resonance. The acquisition process may be monitored via the ***status*** field of the telemetry (see **5.4.1**). On power-up, the ***status*** begins at 8 (oven warm-up). The ***status*** value decrements numerically through the acquisition until normal operation (***status***=0) is achieved.

[1] R. Lutwak, et. al., "The Chip-Scale Atomic Clock – Low-Power Physics Package", *Proceedings of the 36th Annual Precise Time and Time Interval (PTTI) Systems and Applications Meeting*, December 7-9, 2004, Washington, DC.

[2] R. Lutwak, et. al., "The MAC – A Miniature Atomic Clock", *Proceedings of the 2005 Joint IEEE International Frequency Control Symposium and Precise Time & Time Interval Systems & Applications Meeting*, August 29-31, 2005, Vancouver, BC.

4.2 BUILT-IN TEST EQUIPMENT (BITE)

LN CSAC state-of-health can be monitored electronically on Pin 6 (**BITE**) of the LN CSAC. Frequency lock is indicated both by ***status***=0 in the status field of telemetry and by the electrical state of the **BITE** ($\overline{\text{LOCK}}$) output pin, which is high (logic 1) upon initial power-on and whenever ***status*** $\neq 0$. The **BITE** pin is a high-impedance CMOS logic output.

At the conclusion of the acquisition sequence, **BITE** remains high for 5 seconds after ***status***=0 in order to avoid false indication in the event of acquisition failure. Subsequently, **BITE** provides an immediate (within 1 second) indication of lock failure or alarm.

The behavior of **BITE** is identical when operating in ULP mode (see **Error! Reference source not found.**), i.e. it indicates the state of the atomic frequency lock. In ULP, **BITE**=1 during "sleep" periods and reacquisition, and transitions to **BITE**=0 when the LN CSAC is "awake," beginning 5 seconds after ***status***=0.

4.3 10 MHZ OUTPUT CHARACTERISTICS

The 10 MHz sine wave output is provided on Pin 3 of the LN CSAC. The output is capable of driving a 50 ohm load impedance.

The 10 MHz output appears on Pin 3 as soon as the LN CSAC is powered on and is always present, regardless of the lock status. When the LN CSAC is out of lock (**BITE**=1, ***status*** $\neq 0$), the output frequency is provided by the free-running OCXO. Typically, the unlocked frequency accuracy during acquisition is significantly better than this (<1 part in 10^8) as the LN CSAC memorizes its last-known-good tuning voltage and restores this voltage upon power-up and/or subsequent recovery from loss-of-lock.

4.4 FREQUENCY STEERING

For external steering and/or calibration, the LN CSAC internal microwave synthesizer may be adjusted by the user via the RS232 "**!F**" command (see **5.4.2**). Steering values are entered in (integer) units of parts in 10^{15}, though the resolution realized by the LN CSAC hardware is approximately 1 part in 10^{12}. Steering commands may be entered as either *Absolute* steers ("**!FA**") or as *Relative* steers ("**!FD**"). In the case of an absolute steer, the contents of the steer register are replaced with the new value. In the case of a relative steer, the new value is summed with the existing value in the steer register. In either case, the maximum steer that can be entered in a single "**!F**" command is +/- 2 parts in 10^8 (+/- 20000000 pp10^{15}). If a larger correction is sent to the LN CSAC, the maximum allowed steer will be applied. The maximum total steering (including cumulative relative steering commands) is also limited at +/- 2 parts in 10^8, i.e. if a number of relative steers are applied such that the total steering exceeds +/- 2 parts in 10^8 the total steering will be clamped to the maximum correction.

Note that steering commands may be entered during acquisition (**Status** $\neq 0$) but will not take effect until lock is achieved.

Frequency steering is volatile. Upon reboot, the LN CSAC returns to its nominal (calibrated) frequency setting. To update the non-volatile calibration, use the frequency **Latch** command (see **4.5**).

The current steering value appear in the telemetry string as "**Steer**". Note that **Steer** reports the actual hardware steering, in units of pp 10^{12}, even though the software registers maintain resolution of pp 10^{15}, so that many small relative corrections may be applied. As a result, the reported value may appear to disagree with the applied correction by one unit or so due to roundoff error. An example is provided in **5.4.2**.

To apply a frequency correction from the main panel of **CSACdemo**, select **Relative** or **Absolute** from the pulldown menu and enter the desired steering into the **Adjust** field in pp10^{15}.

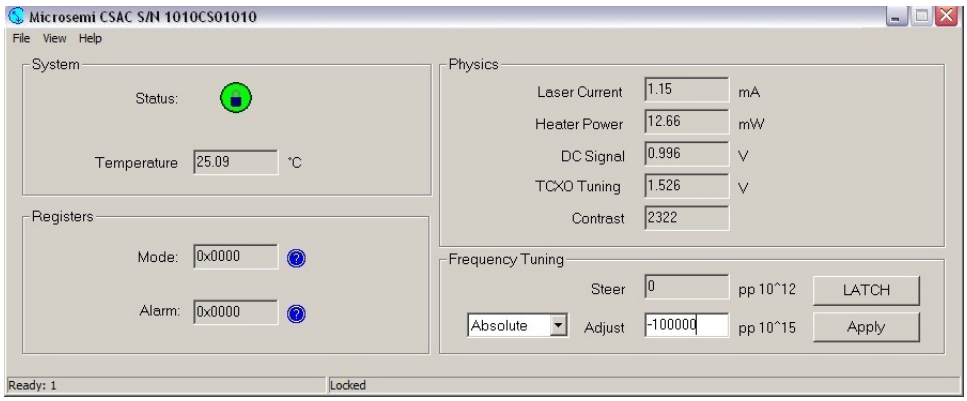

Figure 9: Frequency Offset Adjust

Figure 9 shows an example where an absolute correction of $-1x10^{-10}$ has been entered (as -100000 $pp10^{15}$). The correction is applied to the LN CSAC when you then click on the **Apply** button.

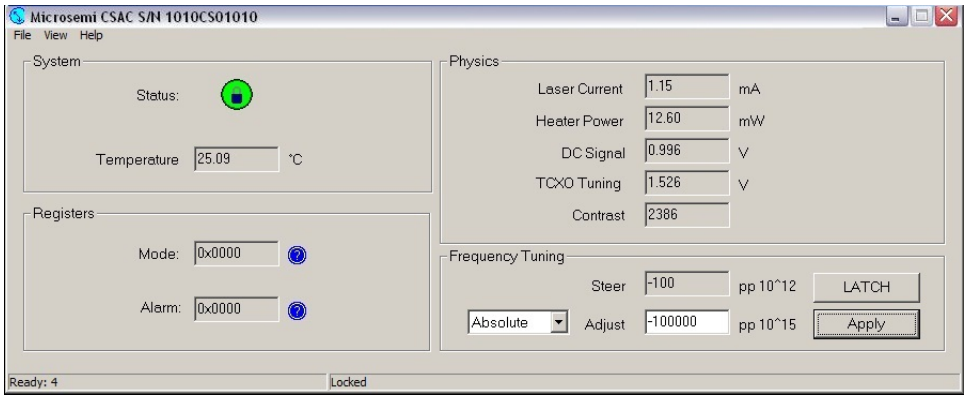

Figure 10: Absolute frequency offset of -1 part in 10^{10} after Apply

As shown in **Figure 10**, after the **Apply** button has been pressed, the correction is applied to the LN CSAC and the value of **Steer** changes (on the next polling update) to indicate the internal correction of $-1x10^{10}$ (as -100 $pp10^{12}$).

Figure 11 below shows an example of relative frequency tuning after absolute steer had been reset to 0. In this example, each time the **Apply** button is clicked, an additional correction of $-1x10^{-10}$ (-100000 $pp10^{15}$) is applied to the LN CSAC. In the screenshot of **Figure 11** the **Apply** button has been clicked a total of four times.

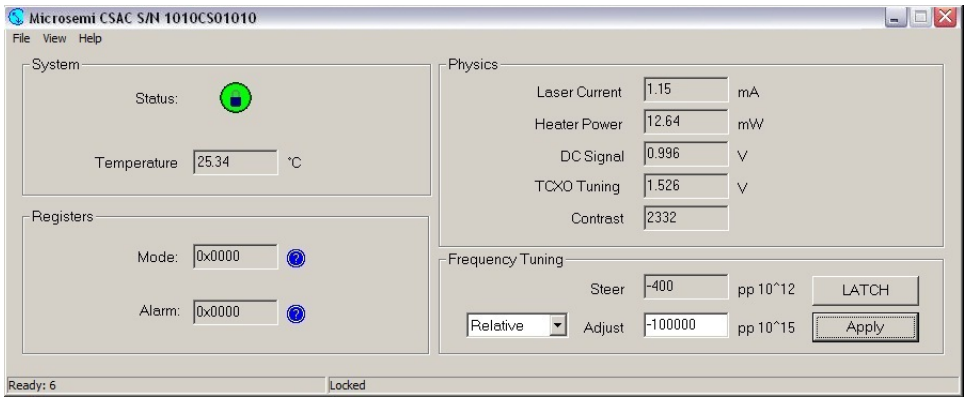

Figure 11: Frequency offset after Applying four relative corrections of -1 part in 10^{10}

4.5 FREQUENCY CALIBRATION

The internal frequency calibration of the LN CSAC is set prior to shipment. It is often desirable (and likely) that the calibration will need to be updated from time to time to remove cumulative frequency aging offsets.

Calibration of the LN CSAC is a two-step process. First, the LN CSAC is **Steer**ed onto frequency, either via an external "**!F**" command (see **4.4**) or through 1 PPS disciplining (see **4.8**). Second, the present value of **Steer** is summed into the non-volatile calibration register via the RS232 frequency **Latch** command ("**!FL**" see **5.4.2**). Following a **Latch** command, the value of **Steer** is reset to zero. Note that the **Latch** command is only valid when the LN CSAC is locked (**Status** = 0).

To **Latch** the current steer value to non-volatile storage from **CSACdemo**, press the **LATCH** button.

Warning: It may be tempting, particularly in disciplining applications, to frequently **Latch** the steering value into calibration, in the event of unforeseen power outage. This is **HIGHLY DISCOURAGED** and **BAD** for the following reason. There is a physical limit on the number of times the non-volatile memory may be written before **DAMAGE** (10,000). If the non-volatile memory of the LN CSAC is updated more than 10,000 times, the LN CSAC may become **INOPERABLE**.

4.6 1 PPS OUTPUT

A CMOS level 1 pulse-per-second (1 PPS) output is available on Pin 10 immediately upon power up. The output series impedance is 200Ω. **Error! Reference source not found.**Nominal levels are 0-3.3 VDC. For synchronization purposes, the "on-time" point is the RISING edge of Pin 10.

The 1 PPS output is derived by digital division of the RF reference frequency. The frequency stability and accuracy of the 1 PPS output therefore reflects that of the RF output. Consequently, when unlocked (**BITE**=1, ***status*** $\neq 0$) the 1 PPS stability reflects that of the free-running OCXO.

4.7 1 PPS SYNCHRONIZATION

The 1 PPS output is synchronous with one rising edge of the 10 MHz output (Pin 3). The 1 PPS output may be synchronized with a *particular* cycle of the 10 MHz output by applying a synchronization pulse to Pin 9. When synchronized, the counters are reset such that the 1 PPS output occurs on the 10 MHz rising edge which is nearest to the externally-applied rising edge. In this fashion, the LN CSAC 1 PPS can be synchronized to within one clock cycle (+/- 100 ns) of the external reference.

The LN CSAC provides two modes for 1 PPS synchronization, "**Manual**" and "**Automatic**", which are selected via a bit in the **Mode Register** (see **Section 5.4.3**). Note that the configuration of the **Mode Register** is non-volatile, i.e. preserved across power cycles.

4.7.1 Manual Synchronization

In **Manual Synchronization** mode (default), the LN CSAC ignores any signal present on the 1 PPS input line (Pin 9) until commanded via RS232. When a synchronization command, "**!S**" (see **5.4.4**), is received, the LN CSAC 1 PPS is synchronized to the next rising edge to appear on Pin 9.

This mode is applicable to configurations where the LN CSAC is embedded in a system where a 1 PPS signal is always present, but not always reliably accurate or stable (such as a GPS receiver). The host microprocessor may command the LN CSAC to synchronize after it has verified the state-of-health of the 1 PPS reference source (e.g. after querying lock state of the GPS receiver).

To perform manual synchronization from **CSACdemo**, open the **1 PPS…** panel from the **View** menu. The **1 PPS** panel is shown below in **Figure 12**.

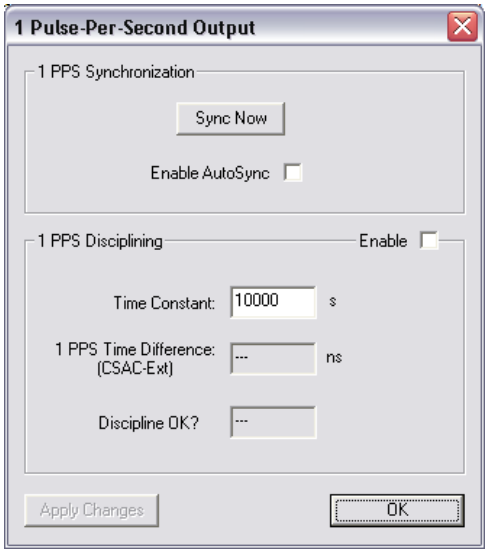

Figure 12: CSACdemo 1 Pulse-per-second Output panel

To manually synchronize the LN CSAC from **CSACdemo**, make sure that a valid 1 PPS reference is connected to the 1 PPS reference input and click on the **Sync Now** button on the **1 PPS** panel. The LN CSAC will synchronize to the next rising edge detected on the 1 PPS reference input.

4.7.2 Automatic Synchronization

In **Automatic Synchronization** mode, the LN CSAC will synchronize its 1 PPS output to *every* rising edge which appears on Pin 9. In this mode, synchronization may be performed by connecting a reference 1 PPS signal to Pin 9 without needing to issue the RS232 synchronization command. Automatic synchronization may be enabled/disabled bit 3 (0x0008) in the **Mode Register** (see **5.4.3**).

This mode may be useful, for example, in cases where the host system does not communicate with the LN CSAC or in which the host system has no method or need to determine the state-of-health of the reference source.

Note that **Automatic Synchronization** mode and **Disciplining** mode (see **4.8**) are mutually exclusive. Enabling either in the **Mode** register will disable the other.

To enable **Automatic Synchronization** from **CSACdemo**, check the **Enable Autosync** checkbox on the **1 PPS** panel and **Apply Changes** (see **Figure 12**).

4.8 1 PPS DISCIPLINING

A high-resolution phase meter is implemented within the LN CSAC for improved synchronization (< 100 ns) as well as for frequency calibration of the LN CSAC, The phase meter measures the time difference between the internal LN CSAC 1 PPS (Pin 10) and the externally applied reference 1 PPS (Pin 9). The phase meter measures the relative phase between the LN CSAC and the reference once per second with a resolution of 450 ps.

Based on the measurements of the phase meter, internal steering algorithms adjust the frequency of the LN CSAC's microwave synthesizer so as to simultaneously steer both the phase and frequency to that of the external reference, ultimately achieving accuracies of < 5 ns and 5 x 10^{-13}, respectively.

Disciplining may be enabled/disabled via bit 4 (0x0010) in the **Mode Register** (see **5.4.3**). The time constant of the steering algorithm is user selectable via the "**!D**" command (see **5.4.5**). Note that both the mode setting and the time constant are non-volatile, i.e. preserved across power cycles.

Prior to the onset of steering, the disciplining algorithms first perform an initialization sequence in which the variables of the steering algorithm are reset to defaults and a 1 PPS synchronization operation (see **4.7**) is executed to bring the 1 PPS output within 100 ns of the reference, thereby avoiding large frequency excursions. Initialization is performed when **Disciplining** is first enabled in the **Mode Register** and, in the case where **Disciplining** is already enabled, immediately after the LN CSAC achieves frequency lock (**BITE**=0, ***status***=0).

In the event that the 1 PPS reference is removed from Pin 9 while **Disciplining**, the LN CSAC remains in "holdover" and preserves the most recent steering value. If the 1 PPS reference subsequently reappears, **Disciplining** will continue where it left off, without reinitializing. The notable exception to this the case in which the LN CSAC 1 PPS has drifted significantly in phase (> 1 μs) from the reference 1 PPS during the outage, in which case a synchronization is performed, though the **Disciplining** variables are *not* reinitialized.

If it is necessary to force reinitialization of the disciplining variables, perhaps because the reference source is subsequently deemed untrustworthy and subsequently recovers, this may be accomplished by disabling and re-enabling **Disciplining** in the **Mode Register** (see **5.4.3**).

When **Disciplining** is enabled, the most recent phase meter measurement, rounded to the nearest nanosecond, is reported in the standard telemetry (see **5.4.1**). The sign of the reported value reflects the measurement of (1PPS_LN CSAC – 1PPS_EXT), i.e. if the LN CSAC 1PPS rising edge occurs prior to the external 1PPS rising edge, then the sign is negative.

The status of **Disciplining** is indicated by the **DiscOK** parameter in the telemetry (see **5.4.1**). **DiscOK**=0 upon startup. **DiscOK**=1 when the magnitude of the phase measurement is < 20 ns for two time constants of duration. **DiscOK**=2 when in holdover (disciplining enabled but no 1 PPS present).

Note that **Automatic Synchronization** (see **4.7.2**) mode and **Disciplining** mode are mutually exclusive. Enabling either in the **Mode** register will disable the other.

In **CSACdemo**, enabling/disabling **Disciplining** and setting the discipline time constant are both accomplished on the **1 PPS** panel, accessible from the **View** menu (See **Figure 12**). To modify the discipline time constant, enter the new value in the field (10-10000) and **Apply Changes**.

4.8.1 Cable length Compensation

The "zero point" of disciplining may be adjusted to accommodate cable and other instrumentation delays (or advances) which impact the arrival time of the 1 PPS at the LN CSAC 1 PPS input pin. The compensation value may optionally be stored in the LN CSAC non-volatile RAM for one-time calibration.

The maximum compensation adjustment is +/- 100 ns, with resolution of 100 ps. The compensation value is entered into the LN CSAC as a signed integer in units of 100 ps, where positive sign indicates phase advancement of the input 1 PPS. For example, if there is 45 ns of delay between the on-time point and the LN CSAC 1 PPS input (approximately 33 feet of RG-58 coaxial cable) then the compensation value would be +450.

Note that cable length compensation can also be employed to correct for dynamic *known* errors in the 1 PPS reference provided, for example, from an external measurement system. For this reason, upon application the compensation is subsequently applied to the *previous* 1 PPS measurement.

Note that compensation is implemented in the disciplining algorithm, not in the phase measurement itself. The phase measurement, as reported via telemetry, reports the actual phase measurement, i.e. if the LN CSAC is disciplined with +50 ns of compensation, the phase meter will report -50 ns of phase error.

Compensation is set with the "**!DC**" command (see **5.4.6**).

4.8.2 The "Art" of Disciplining

Implemented correctly, disciplining can be utilized to calibrate the LN CSAC frequency in the field, even if a reference source is only occasionally or sporadically available, thereby improving the long-term performance (phase and frequency drift) of the LN CSAC. At the same time, the disciplined LN CSAC may be used to "clean-up" the short-term stability of an accurate, but noisy, reference source, such as GPS.

Implemented incorrectly, however, disciplining may degrade the performance of the LN CSAC if, for example, the LN CSAC is disciplined with a short time constant to a source which is itself noisier than the LN CSAC, such as GPS.

Implementing a successful disciplining strategy involves understanding the noise properties of the LN CSAC, the reference source, and the phase meter itself, and selecting the appropriate time constant that makes the best use of the available timing information.

4.9 TIME-OF-DAY

The LN CSAC maintains time-of-day (TOD) as a 32-bit unsigned integer which is incremented synchronously with the rising edge of the 1 PPS output. Until set otherwise, TOD begins counting from zero when the LN CSAC is powered on.

TOD is retrieved from the LN CSAC over RS232 with the "**!T?**" command (see **5.4.8)**. When the "**!T?**" command is received, the LN CSAC waits for the next rising edge of 1 PPS before replying with the TOD of the current epoch, i.e. if the command is received during epoch ***N***, then the reply "***N+1***" appears immediately following the next 1 PPS. This strategy provides the host system with minimum ambiguity in interpreting the response.

TOD may be set with the "**!T**" command via the RS232 interface (see **5.4.8)**. The "**!T**" command includes provision both for setting an absolute number or for a differential (+/-) adjustment of the present TOD. An example is provided in **5.4.8**. In order to avoid ambiguity in *setting* the TOD, it is recommended that the host system wait for 1 PPS and transmit the setting/adjustment immediately thereafter.

The **CSACdemo** program shows TOD on the **Time-Of-Day…** panel, accessed from the **View** menu and shown below in **Figure 13**.

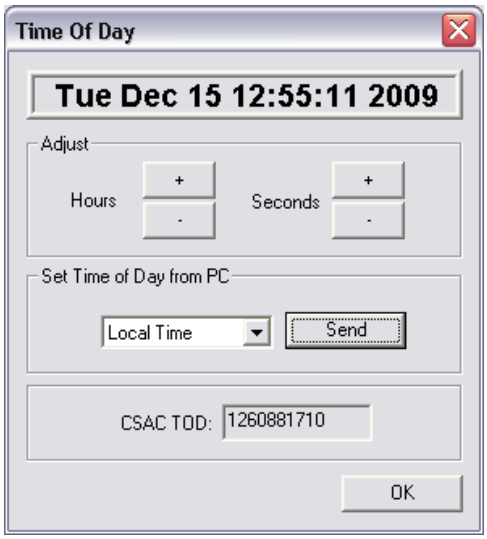

Figure 13: CSACdemo Time-Of-Day panel

The "raw" LN CSAC TOD value is shown in the lower field of the panel (here 1260881710). The upper display of the TOD panel realizes the time-keeping convention of the C Programming language (as well as in UNIX and Microsoft Windows®) which counts time in seconds from midnight on January 1, 1970. If you click on the **Send** button, it will set the LN CSAC time according to the host PC's TOD counter (either local time or UTC depending on the setting of the pull-down menu to the left of the **Send** button). The **+** and **–** Hours and Seconds buttons increment or decrement the LN CSAC TOD by +/- 3600 or +/-1 second respectively.

4.10 ANALOG TUNING

Analog Tuning is not a feature that is available on the LN CSAC. It is available as a menu item on **CSACdemo** to support Microsemi's standard CSAC products such as the SA.45s, but should be ignored for use with LN CSAC. Toggling Analog Tuning controls will cause the LN CSAC to lose lock but will not damage the device.

5 PROGRAMMER'S REFERENCE

5.1 RS232 HARDWARE INTERFACE

Pins 7 and 8 provide a serial interface for communication with the LN CSAC. The protocol is fundamentally similar to RS232, with the exception that the voltage levels are CMOS (0-VCC), rather than +/- 12 V. The serial interface operates at 57600 Baud, 8 data bits, No Parity, and 1 Stop Bit (8-N-1) with no flow control. For interfacing with a standard RS232 controller interface, which requires +/- 12 V logic levels, an external level shifter must be employed, such as the **Maxim MAX202** employed on the **Evaluation Board** (see Figure 1).

5.2 OVERVIEW OF TELEMETRY INTERFACE

The LN CSAC communicates exclusively with printable (non-binary) ascii characters.

In general, commands are to be preceded by an exclamation point ("**!**") and followed by a carriage-return/linefeed **[CRLF]** pair (ascii 0x0D 0x0A). For convenience and efficiency, most commands also provide a single-character shortcut, which is executed immediately, i.e. without bracketing by '**!**' and **[CRLF]**. For example, the single character shortcut '^' is functionally identical to "**!^[CRLF]**".

After transmitting '**!**' but prior to sending **[CRLF]**, a command may be aborted by sending the escape character (ascii 0x1B).

All commands produce a response from the LN CSAC which are human readable, with individual lines ending in **[CRLF]**. If an unsupported or improperly formatted command is received, the LN CSAC responds with "?**[CRLF]**".

5.2.1 Checksum

For improved communications reliability, an NMEA-style checksum may be enabled via bit 6 (0x0040) of the **Mode Register** (see **5.4.3**). When enabled, the checksum is required for all input commands and is present on all replies from the LN CSAC.

The checksum is a two-byte Ascii representation (in hexadecimal) of the XOR of all characters in the command between – but not including – the **!** and the **[CRLF]** characters. The checksum is preceded by a '*****' character and appended to the command immediately prior to the **[CRLF]**. Because commands including checksum are inherently multi-character, single-character shortcuts are not available when checksum is enabled.

Example (Disable checksum via **Mode** register):

Command:	**!Mc*2E[CRLF]**
Unit Response:	**0x0000[CRLF]**

If the checksum is not present or if the checksum value is invalid, then the command is not executed and the LN CSAC responds with "***[CRLF]**".

Example (Malformed checksum):

Command:	**!Mc*2D[CRLF]**
Unit Response:	***[CRLF]**

To experiment with checksum in **CSACdemo** and observe the calculated checksums in the **Trace** window, enable the **Require Cksum** checkbox on the **Options…** panel (see **Figure 4**).

5.3 COMMAND SUMMARY

Table 2, below, summarizes the LN CSAC commands. The single-character shortcut equivalents are defined in Column "**shortcut**". Column "**Ref. Section**" refers to detailed descriptions in sections **5.4.*x*** below.

Cmd	Description	Shortcut For	Ref. Section
6	Return telemetry headers as comma-delimited string	**!6[CRLF]**	**5.4.1**
^	Return telemetry as comma-delimited string	**!^ [CRLF]**	**5.4.1**
F	Adjust frequency	**!F?[CRLF]**	**5.4.2**
M	Set operating mode register bits	**!M?[CRLF]**	**5.4.3**
S	Sync LN CSAC 1 PPS to external 1 PPS	**!S[CRLF]**	**5.4.4**
D	Set 1 PPS disciplining time constant	**!D?[CRLF]**	**5.4.5**
U	Set ultra-low power mode parameters	**!M?[CRLF]**	**5.4.7**
T	Set/report time-of-day	**!T?[CRLF]**	**5.4.8**
?	Help	**!?[CRLF]**	**5.4.10**

Table 2: LN CSAC command summary

5.4 DETAILED COMMAND DESCRIPTIONS

5.4.1 Telemetry (6 and ^)

LN CSAC supports two commands, "**!6**" and "**!^**" to retrieve the telemetry headers and values, respectively. Both responses are comma-delimited strings, suitable for importing into spreadsheet programs.

Telemetry headers command: **!6[CRLF]**

Unit Response: Comma-delimited string of identifiers ending in carriage return/linefeed

Example Response:

Status, Alarm,SN,Mode,Contrast,LaserI,OCXO,HeatP,Sig,Temp,Steer,ATune,Phase,DiscOK,TOD,LTime,Ver[CRLF]

Telemetry data command: **!^[CRLF]**

Unit Response: Comma-delimited string of telemetry data ending in carriage return/linefeed

Example Response:

0,0x0000,1209CS00909,0x0010,4381,0.86,1.573,17.62,0.996,28.26,-24,---,-1,1,1268126502,586969,1.0[CRLF]

Note that the single-characters '**6**' and '**^**' are shortcuts for "**!6[CRLF]**" and "**!^[CRLF]**", respectively.

Table 3, below, lists the telemetry parameters and their associated header identifiers.

Identifier	Description	Notes
Status	Unit Status	*See Note 1*
Alarm	Pending Unit Alarms	*See Note 2*
SN	Unit serial number	*See Note 3*
Mode	Mode of operation	see **5.4.3** for bit definitions.
Contrast	Indication of signal level	Typically > 2000 when locked, and ≈0 when unlocked.
LaserI	Laser current (mA)	Typically 0.6 – 1.3 mA
OCXO	Tuning Voltage (V)	0-2.5 VDC tuning range ≈ ±10 ppm
HeatP	Physics package Heater Power (mW)	Typical 6-20 mW under normal operating conditions and 25°C ambient
Sig	DC Signal Level (V)	Typical 0.8 – 1.7V under normal operating conditions
Temp	Unit temperature (°C)	Absolute accuracy is +/- 2°C
Steer	Frequency adjust	In $pp10^{12}$
Phase	1PPS_LN CSAC-1PPS_EXT (ns)	Only present when disciplining enabled, otherwise "**---**"
DiscOK	Discipline status (0-2)	'**0**'=acquiring, '**1**'=locked, '**2**'=holdover when disciplining enabled, otherwise "**---**"
TOD	Time (seconds)	Starts at 0 upon powerup unless set by command
LockT	Time since lock (seconds)	Starts at 0 upon lock
FWver	Firmware version	Two digit number "***M.m***" where '***M***' is major revision and '***m***' is minor revision.

Table 3: Telemetry parameters

Note 1: **Status** reflects the steps of the clock initialization process. It starts at 8 on boot and decreases to 0 as acquisition proceeds. When **Status** ≠0, **BITE**=1. When **Status** =0, **BITE** =0.

Status	Acquisition stage
9	Asleep (ULP mode only)
8	Initial warm-up
7	Heater equilibration
6	Microwave Power Acquisition
5	Laser Current Acquisition
4	Laser Power Acquisition
3	Microwave Frequency Acquisition
2	Microwave Frequency Stabilization
1	Microwave Frequency Steering
0	Locked

Table 4: Status register and acquisition stages

Note 2: Alarms indicate detection of anomalous operating conditions while locked. **Alarm** is the logical OR of all pending alarms (see **Table 5**). If any alarm is tripped (**Alarm ≠ 0x000)**, the LN CSAC will return to **Status** = 8.

Alarm	Definition	Alarm Limit
0x0001	Signal Contrast Low	Contrast < 1000
0x0002	Synthesizer tuning at limit	Synthesizer detuned from calibration by > +30 kHz or < -15 kHz
0x0004	Temperature Bridge Unbalanced	Bridge – Setpoint > +/- 20 mV
0x0010	DC Light level Low	Setpoint – DCL > 1.5V
0x0020	DC Light level High	DCL – Setpoint > 1.5V
0x0040	Heater Voltage Low	< 30 mV
0x0080	Heater Voltage High	> 2.48 V
0x0100	uW Power control Low	< 20 mV
0x0200	uW Power control High	> 2.48 V
0x0400	OCXO control voltage Low	< 0.1 V
0x0800	OCXO control voltage High	> 2.4 V
0x1000	Laser current Low	< 0.5 mA
0x2000	Laser current High	> 2.3 mA
0x4000	Stack overflow (firmware error)	

Table 5: Alarm definitions

Note 3: LN CSAC serial numbers are of the form YYMMCSXXXXX where YYMM is the year and month of production and XXXXX is the serialized production unit number.

5.4.2 Frequency Adjustment (F)

The output frequency of the LN CSAC may be adjusted (steered) via RS232. The internal resolution of the fractional frequency correction is approximately 1 part in 10^{12}. The correction is entered as integer parts in 10^{15}. The maximum allowed correction, in a single command, is ±20000000 (2 parts in 10^{8}). Corrections may be applied as either **Absolute** or **Relative**, depending on the first character following the "**!F**", i.e. "**!FA**" or "**!FD**" for absolute or relative ("delta") respectively. In the case of absolute steering, the value of the **Steer** register is replaced with the new value. In the case of relative (delta) steering, the new value is summed with the existing value in the **Steer** register, i.e. two relative corrections of -10000 result in a total offset of $-2x10^{-11}$. The current steering value is reported in the **Steer** field of the telemetry in units of $pp10^{12}$.

Adjust frequency command: **!F*YXXXXX*[CRLF]** *where **Y** is either '**A**' or '**D**' and **XXXXX** is the new correction in parts in 10^{15}.*

Example (Apply absolute tuning correction of $-1.23x10^{-10}$):

Command: **!FA-123000[CRLF]**

Unit Response: **Steer = -123[CRLF]**

Example (Apply delta tuning correction of $-1.23x10^{-10}$):

Command: **!FD-123000[CRLF]**

Unit Response: **Steer = -246[CRLF]**

Example (Report current value of **steer**):

Command: **!F?[CRLF]**

Unit Response: **Steer = -246[CRLF]**

Note that the single-character '**F**' is a shortcut for "**!F?[CRLF]**".

The contents of the **Steer** register are volatile, i.e. the **Steer** is reset to 0 when power is cycled to the LN CSAC. In many cases it is desirable to preserve the steer upon power-down, e.g. for calibration of the LN CSAC. This is accomplished by sending a **Frequency Latch** command to the LN CSAC, which updates the internal calibration

(stored in non-volatile memory) according to the current value of the **Steer** register and resets **Steer** to zero. Note that the **Latch** command is only valid when the LN CSAC is locked (**Status** = 0).

Latch calibration value: **!FL[CRLF]**

Example:

Command: **!FL[CRLF]**

Unit Response: **Steer Latched [CRLF]**
Steer = 0[CRLF]

WARNING: The frequency steering command (**!F**) is recommended for real-time disciplining of LN CSACs, but the value should NOT be latched (**!FL**) on every steer due to the physical limit on the number of times the non-volatile memory may be written before damage (10,000). For example, if an **!FL** command was applied to the LN CSAC, accompanying a steer (**!F**), at a rate of 1/sec, the LN CSAC is expected to fail within 4 hours.

5.4.3 Set/clear Operating Modes (M)

Operating modes of the LN CSAC are enabled/disabled via individual bits in the **Mode** register. The **!M** command provides access to set/clear each of the bits independently. The **Mode** register is non-volatile, i.e. settings persist across power cycles.

The unit responds by reporting the current value of the mode register in hexadecimal. Each bit in the mode register is associated with enabling/disabling a particular operating mode. The bit assignments are:

0x0001	Reserved
0x0002	Reserved
0x0004	Reserved
0x0008	1 PPS auto-sync enable
0x0010	Discipline enable
0x0020	Ultra-low power mode enable
0x0040	Require checksum on ! command
0x0080	Reserved

The arguments to the **!M** command include:

S/s	Enable/disable 1 PPS auto-sync
D/d	Enable/disable 1 PPS disciplining
U/u	Enable/disable ultra-low power mode
C/c	Enable/disable NMEA-style checksum
?	Report current settings

Example (Enable and then Disable 1 PPS auto-sync):

Command: **!MS[CRLF]**

Unit Response: **0x1000[CRLF]**

Command: **!Ms[CRLF]**

Unit Response: **0x0000[CRLF]**

The current value of the mode register is returned in the standard telemetry query (see **5.4.1**) or may be queried independently with the "**!M?**" command.

Example (query Mode register):

Command: **!M?[CRLF]**

Response: **0x0001[CRLF]**

Note that the single-character '**M**' is a shortcut for "**!M?[CRLF]**".

Autosync mode and **D**iscipline mode are mutually exclusive. Setting one will automatically disable the other.

5.4.4 1 PPS Synchronization (S)

In order to synchronize the 1 PPS output (Pin 10) to an externally applied 1 PPS synchronization input (Pin 9), connect the 1 PPS input to Pin 9 and send the "**!S**" command. The rising edge of the 1 PPS output will be synchronized to within +/- 100 ns of the next rising edge of the 1 PPS input. If a valid 1 PPS input does not appear at the 1 PPS input within 3 seconds, the operation is aborted and an error is returned.

Synchronize 1PPS: **!S[CRLF]**

Unit Response: **S[CRLF]** *or* **E[CRLF]**

The unit response (**S** or **E**) occurs *after* either successful synchronization or 3-second timeout. This permits the host system to verify successful synchronization.

Note that the single-character '**S**' is a shortcut for "**!S[CRLF]**".

5.4.5 Set 1 PPS Disciplining Time Constant (D)

The time constant for disciplining to an externally-supplied 1 PPS reference source may be selected to provide optimal performance in a given application (see **4.8.2**). The time constant can lie in the range of 10 to 10000 seconds.

The 1 PPS disciplining time constant is set with the **!D** command:

Set Time Constant command: **!D*X*[CRLF]** *where **X** is the new time constant in seconds.*

Example (set disciplining time constant to 80 seconds):

Command: **!D80[CRLF]**

Response: **80[CRLF]**

To query the current time constant setting, without modifying the value, use the command "**!D?**"

Example (query current disciplining time constant):

Command: **!D?[CRLF]**

Response: **80[CRLF]**

Note that the single-character '**D**' is a shortcut for "**!D?[CRLF]**".

5.4.6 Set 1 PPS Disciplining Cable Length Compensation (DC)

Cable length compensation can be applied to allow for known delay (or advance) in the arrival time of the reference 1 PPS at the LN CSAC (see **4.8.1**).

Cable length compensation is represented as a signed integer in units of 100 ps, with a maximum value of +/- 1000 (100 ns). The sign of the compensation is such that a positive value reflects known *DELAY* in the arrival time of the 1 PPS, i.e. 33 feet of RG-58 cable requires compensation of +50 ns.

The cable length compensation value is set with the **!DC** command:

Set Time Constant command: **!DC*X*[CRLF]** *where **X** is the new compensation value*

Example (set cable length compensation to +15 nanoseconds):

Command: **!DC150[CRLF]**

Response: **150[CRLF]**

To query the current compensation setting, without modifying the value, use the command "**!DC?**"

Example (query current compensation setting):

Command: **!DC?[CRLF]**

Response: **150[CRLF]**

To store the current compensation setting in non-volatile RAM, use the command "**!DCL**"

Example (Latch current value of compensation to power-up default):

Command: **!DCL[CRLF]**

Response: **Phase comp latched[CRLF]**

5.4.7 Set Ultra-low Power Mode Parameters (U)

The ultra-low power operating mode is defined by two parameters, "**Sleep-Time**" and "**Wake-Time**", which may be set with the **!U** command.

Set ULP parameters command: **!U*SSS*,*WWW*[CRLF]**

*where **SSS** is the sleep time in seconds and **WWW** is the wake-time in seconds.*

Example (set sleep-time=55 minutes, wake-time=5 minutes):

Command: **!U3300,300[CRLF]**

Response: **3300,300[CRLF]**

The allowed ranges of **Sleep-Time** and **Wake-Time** are 1800-65535 seconds and 10-65535 seconds, respectively.

To query the ULP settings, without modifying their values, use the command "**!U?**"

Example (query current ULP settings):

Command: **!U?[CRLF]**

Response: **3300,300[CRLF]**

Note that the single-character '**U**' is a shortcut for "**!U?[CRLF]**".

5.4.8 Time-of Day (T)

Time-of-day (TOD) is maintained internally within the LN CSAC, represented by a single unsigned long integer value, which begins counting up from 0 when the LN CSAC achieves lock. The TOD is synchronized with the 1 PPS output. TOD is routinely transmitted in the telemetry string (see **Table 3**).

TOD may be set externally with the **!T** command:

Set TOD command: **!T*Y XXXX*[CRLF]**

*where **Y** is either '**A**' for absolute setting or '**D**' for a delta adjustment of TOD*

*and **XXXX** is either the unsigned integer TOD (typically either UNIX/Windows time or GPS time) or a signed integer adjustment to the TOD.*

Example (Absolute setting TOD to 1221578499):

Command: **!TA1221578499[CRLF]**

Unit Response: **TimeOfDay = 1221578499[CRLF]**

Example (retard TOD by 3600 seconds = 1 hour):

Command: **!TD-3600[CRLF]**

Unit Response: **TimeOfDay = 1221574902[CRLF]**

Example (advance TOD by 3600 seconds = 1 hour):

Command: **!TD3600[CRLF]**

Unit Response: **TimeOfDay = 1221574902[CRLF]**

The TOD may be reported synchronous with the 1 PPS output in order to enable unambiguous external time syntonization:

Retrieve TOD command: **!T?[CRLF]**

Unit Response: ***XXXX*[CRLF]** *where **XXXX** is the current TOD.*

Note that this response does not occur until immediately following the next 1PPS output pulse.

When queried with the '**!T?**' command, the first character of TOD will appear on RS232 within 20 ms of the rising edge of the next 1 PPS output pulse. Because this necessarily creates a delay of up to a second between sending the '**!T?**' command and receiving a response from the LN CSAC, the host system must allow for an RS232 receive timeout of at least 1000 ms when anticipating a response to the '**!T?**' command. For less critical timing applications, the TOD can be somewhat ambiguously parsed from the standard telemetry string (see **5.4.1**).

Note that the single-character '**T**' is a shortcut for "**!T?[CRLF]**".

5.4.9 Deferred Command (@)

Any command can be sent at a deferred time by using the **!@** command:

Send deferred command: **!T@*XXXX,YYYY*[CRLF]**

*where **XXXX** is the deferred time in seconds and **YYYY** is the command that will be sent after the deferred time.*

Example (Defer sending the "**6**" command by 10 seconds):

Command: **!@10,6[CRLF]**

Unit Response: **Deferred = 10, "6"**

Unit Response (after 10 seconds):
Status,Alarm,SN,Mode,Contrast,LaserI,OCXO,HeatP,Sig,Temp,Steer,ATune,Phase,DiscOK,TOD,LTime,Ver

Example (Defer sending the **"!T?**" command by 5 seconds):

Command: **!@5,!T?[CRLF]**

Unit Response: **Deferred = 5, "!T?"**

Unit Response (after 5 seconds): **75173**

5.4.10 Help (?)

A list of all available commands is displayed in response to the **?** command.

Display all commands: **?**

Unit Response:

F	**Adjust Frequency**
^	**Telemetry**
6	**Telemetry Headers**
D	**Set 1PPS Discipline Tau**
S	**Sync 1PPS**
U	**Set parameters for ultra-low power mode**
M	**Change Mode register**
T	**Change/Report Time of Day**
?	**Show this list**
@	**Delayed Command Execution**

Note that the single-character '**?**' is a shortcut for "**!?[CRLF]**".