TR0030
Test Report
RTG4 FPGA CoreJESD204BRX Interoperability

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document.

2 RTG4 CoreJESD204BRX Interoperability Test Report

2.1 Introduction

Microsemi provides interfacing solutions for analog-to-digital converter (ADC) and digital-to-analog converter (DAC) devices using the JESD204B JEDEC standards. These solutions are provided as DirectCore soft IPs (CoreJESD204BRX and CoreJESD204BTX) and interfaced with the high-speed serial interfaces (SERDESIF) of RTG4™ FPGA device. This report provides the Interoperability test results performed on a Texas Instruments' ADC device (ADC12J1600EVM) as per JEDEC standards. The interoperability test report describes the JESD204B link parameters, hardware test setup, equipment used, and final test results of Microsemi CoreJESD204BRX.

2.1.1 References

- *CoreJESD204BRX IP Handbook*
- *UG0567: RTG4 FPGA High Speed Serial Interface User Guide*
- *ADC12J1600EVM User Guide*
- *Identify ME User Guide*

2.1.2 Scope

This report describes the hardware setup used for interoperability testing and the test results. The RTG4 JESD204B solution supports link widths of ×1 to ×8 up to 3.2 Gbps per lane using subclass 0 and 1. The following table shows the configuration of the tested device.

Table 1 • **Configuration of the Tested Devices**

Device	Link Rate	Link Width	Subclass
Texas Instruments - ADC12J1600	2 Gbps	×2	0, 1

2.2 Test Requirements

The following are the hardware and software required for interoperability test.

2.2.1 Hardware Requirements

- RTG4 Development Kit (RT4G150-CG1657)
- ADC12J1600EVM Evaluation board
- Low-noise signal generator
- 110 V to 240 V AC to 5-V DC-Power adapter
- 110 V to 240 V AC to 12-V DC-Power adapter
- FlashPro4 programmer
- Two USB A to mini-B cables

2.2.2 Software Requirements

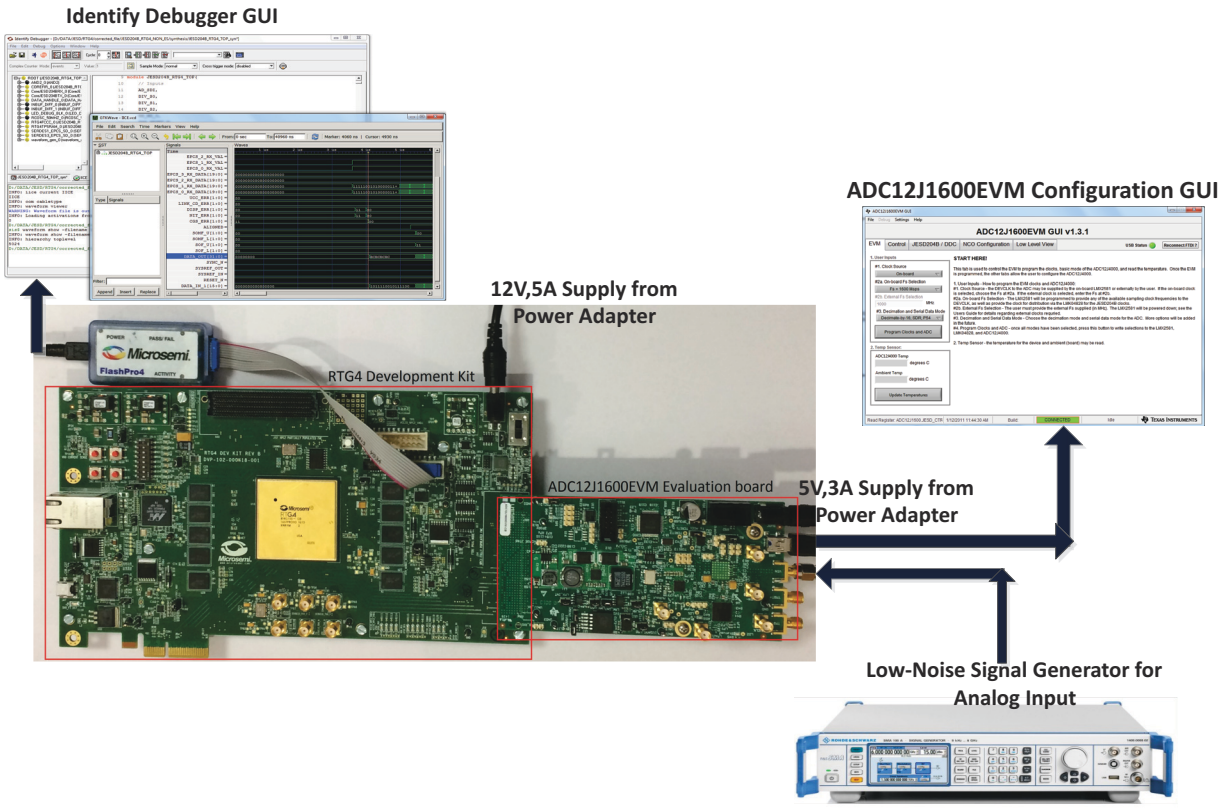
- Libero® System-on-Chip (SoC) software
- ADC12J1600EVM configuration software

2.3 Hardware Setup

The interoperability test was performed on the RTG4 Development Kit (RT4G150-CG1657) and the Texas Instruments' ADC12J1600 FMC card.

The interoperability test design was developed using the Libero SoC software by instantiating the CoreJESD204BRX IP core and other required IP cores in SmartDesign. Texas Instruments' ADC register configuration GUI and Identify Debugger tool were used for the interoperability test. The CoreJESD204BRX IP was configured in JESD204B Subclass 0 and Subclass 1 modes. The following figure shows the hardware setup.

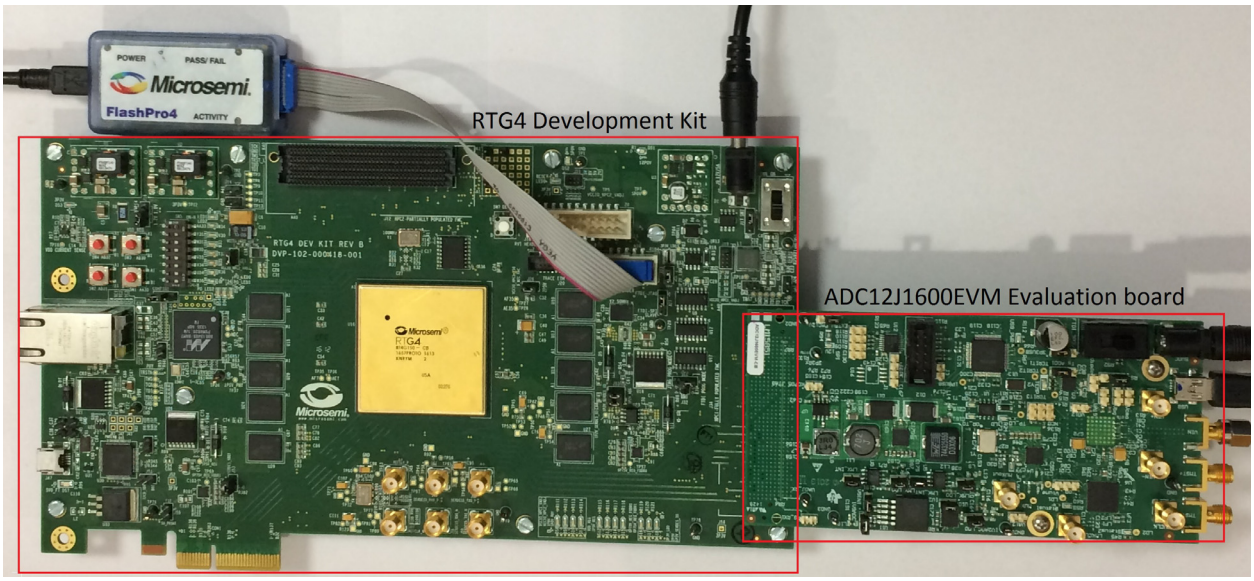
Figure 1 • **Hardware Setup for Interoperability Testing with RT4G150-CG1657 and ADC12J1600EVM**



2.3.1 ADC12J1600EVM Setup

The ADC12J1600 FMC card was connected to the RTG4 Development Kit FMC HPC1 connector. ADC12J1600 was configured in two converters and two-lane mode using ADC12J1600 EVM configuration GUI. Each lane was operated in 2 Gbps mode. The fabric logic and SerDes blocks were operated using 100 MHz frequency. The following figure shows the hardware setup for ADC12J1600EVM.

Figure 2 • **Hardware Setup for Interoperability Testing with ADC12J1600EVM**



2.3.1.1 Interoperability Tests Settings

CoreJESD204BRX and ADC12J1600EVM were configured, as shown in the following table.

Table 2 • **Configuring CoreJESD204BRX and ADC12J1600EVM**

Parameter	CoreJESD204BRX Value	ADC12J1600EVM	Description
SCR	0/1	0×1/0×0	Scramble enable/disable
L	2	0×2	Lanes
F	2	0×2	Octets per frame
K	32	0×1F	Frames per multi-frame
M	2	0×02	Converters
CS	1	0×01	Control bits per sample
N	15	0×0F	Sample resolution
N'	16	0×10	Sample envelope
S	1	0×1	Samples per converter per frame
HD	0	0×0	High density mode
CF	0	0×0	Control bits per frame
SUBCLASSV	0/1	0×0/0×1	0×0/0×1

2.3.2 ADC12J1600EVM Interoperability Tests

The following interoperability tests were performed on CoreJESD204BRX and ADC12J1600EVM:

- Test 1: Data Link Layer - Code group synchronization
- Test 2: Data Link Layer - Initial lane alignment sequence
- Test 3: Receiver transport layer
- Test 4: Descrambling
- Test 5: Deterministic latency

2.3.2.1 Test 1: Data Link Layer—Code Group Synchronization

On link startup, the receiver issues a synchronization request and the transmitter emits comma characters /K/ = /K28.5/. Identify debugger was used to monitor the operation of the receiver data link layer. The following table shows the data link layer—code group synchronization (CGS) test results.

Table 3 • **Data Link Layer—Code Group Synchronization Test Results**

Test Case	Objective	Description	Passing Criteria	Results
TI_ADC1.1	Check if the receiver asserts SYNC_N signal when the link was down.	CoreJESD204BRX_0 -> SYNC_N signal was observed in Identify Debugger.	SYNC_N was low.	Passed.
TI_ADC1.2	Check if SYNC_N request was de-asserted on receiving at least four successive /K/ characters.	CoreJESD204BRX_0 -> DATA_OUT[15:0], DATA_OUT[31:16], and SYNC_N signals were observed in Identify Debugger.	K28.5 or /K/ character (0 × BC) was observed on DATA_OUT and SYNC_N was de-asserted on receiving at least four successive /K/ characters.	Passed.
TI_ADC1.3	Check the full code group synchronization at receiver on receiving another four successive 8B/10B characters.	CoreJESD204BRX_0 -> DATA_OUT[15:0], DATA_OUT[31:16], SYNC_N, and CGS_ERR[1:0] signals were observed in Identify Debugger.	CGS error was not asserted.	Passed.

2.3.2.2 Test 2: Data Link Layer—Initial Lane Alignment Sequence

The following table shows the data link layer—initial lane alignment sequence (ILAS) test results.

Table 4 • **Data Link Layer—Initial Lane Alignment Sequence Test Results**

Test Case	Objective	Description	Passing Criteria	Results
TI_ADC2.1	Check if the ILA phase starts after the CGS phase.	CoreJESD204BRX_0-> DATA_OUT[15:0], DATA_OUT[31:16], SOMF_U[3:0], SOMF_L[3:0], SOF_U[1:0], and SOF_L[1:0] signals were observed in Identify Debugger.	Multi-frame starts with 0×1C and was aligned to SOMF_U[3:0].	Passed.
TI_ADC2.2	Check the JESD configuration data in the second multi-frame.	CoreJESD204BRX_0 -> DATA_OUT[15:0], DATA_OUT[31:16], SOMF_U[3:0], SOMF_L[3:0], SOF_U[3:0], SOF_L[3:0], and LINK_CD_ERROR[3:0] signals were observed in Identify Debugger.	Observe the second multi-frame that starts with 0×1C followed by 0×9C and JESD204B configuration data.	Passed.

2.3.2.3 Test 3: Receiver Transport Layer

The following table shows the receiver transport layer test results.

Table 5 • **Receiver Transport Layer Test Results**

Test Case	Objective	Description	Passing Criteria	Results
TI_ADC3.1	Check data integrity in test mode.	ADC was configured in short/long transport test mode. CoreJESD204BRX_0 -> DATA_OUT[15:0] and DATA_OUT[31:16] signals were observed in Identify Debugger	Observe the DATA_OUT for short/long transport test mode.	Passed
TI_ADC3.2	Check data integrity in normal mode.	ADC was configured in normal mode. CoreJESD204BRX_0 -> DATA_OUT[15:0], and DATA_OUT[31:16] signals were observed in Identify Debugger.	Received signal correlates with the input signal given for ADC sampling.	Passed

2.3.2.4 Test 4: Descrambling

Scrambler was enabled in ADC and descrambler was enabled in CoreJESD204BRX IP. The following table shows the descrambling test results.

Table 6 • **Descrambling Test Results**

Test Case	Objective	Description	Passing Criteria	Results
TI_ADC4.1	Check descrambler functionality	ADC was configured in short/long transport test mode. CoreJESD204BRX _0 -> DATA_OUT[15:0] and DATA_OUT[31:16] signals were observed in Identify Debugger.	Observe the DATA_OUT for short/long transport test mode.	Passed

2.3.2.5 Test 5: Deterministic Latency

2.3.2.5.1 Subclass 1 Mode

CoreJESD204BRX IP and ADC12J1600EVM were configured in Subclass 1 mode. The following table shows the JESD204B deterministic latency measurement test results.

Table 7 • **JESD204B Deterministic Latency Measurement Test Results—Subclass 1 Mode**

Test Case	Objective	Description	Passing Criteria	Results
TI_ADC5.1.1	Check local multi-frame counter (LMFC) alignment.	CoreJESD204BRX_0 -> clkgen_lmfc, and SYSREF_IN signals were observed in Identify Debugger.	SYSREF_IN aligned to clkgen_lmfc.	Passed
TI_ADC5.1.2	SYSREF capture.	CoreJESD204BRX _0 -> c2l_mf_phase, and SYSREF_IN signals were observed in Identify Debugger.	LMFC counter restarts after the SYSREF_IN capture.	Passed

Table 7 • **JESD204B Deterministic Latency Measurement Test Results—Subclass 1 Mode *(continued)***

Test Case	Objective	Description	Passing Criteria	Results
TI_ADC5.1.3	Check latency from start de-assertion of SYNC_N to first user data output.	Check Latency was fixed for every Link reset/initialization.	Latency must be the same for link reset/initialization.	Passed
TI_ADC5.1.4	Check the data latency during user data phase.	Check if the data latency was fixed during the user data phase. CoreJESD204BRX_0 -> DATA_OUT[15:0] and DATA_OUT[31:16] signals were observed in Identify Debugger.	The ramp pattern without distortion.	Passed