TR0033
Test Report
PolarFire FPGA JESD204B Interoperability for AD9371

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 4.0

Updated the document for Libero SoC v12.0 and SoftConsole v6.0.

1.2 Revision 3.0

The following is a summary of changes made in this revision.

- In the Device Requirements table, the link rate information was updated (see Table 1, page 2).
- The Cortex-M1 is replaced with Mi-V in the document.
- The figure, Data Captured in Identify Debugger Tool, is added (see Figure 5, page 5).

1.3 Revision 2.0

The following is a summary of the changes in this revision.

- Updated the AD9371-Transmitter value for F parameter. For more information, see Table 2, page 5.
- Updated the Test 4: Descrambling section. For more information, see Test 4: Descrambling, page 11.

1.4 Revision 1.0

Revision 1.0 was the first publication of this document.

2 PolarFire FPGA CoreJESD204BRX and CoreJESD204BTX Interoperability Test Report for AD9371

Microsemi provides interfacing solutions for analog-to-digital converter (ADC) and digital-to-analog converter (DAC) devices using the JESD204B JEDEC standards. These solutions are provided as DirectCore soft IPs (CoreJESD204BRX and CoreJESD204BTX) in Libero® SoC. These IP cores interface with transceivers of PolarFire FPGA devices. This report provides the results of interoperability tests performed on a third-party ADC and DAC device. The interoperability test report describes the JESD204B link parameters, hardware test setup, equipment used, and final test results of Microsemi DirectCores: CoreJESD204BRX and CoreJESD204BTX.

2.1 References

- *CoreJESD204BRX IP Handbook*
- *CoreJESD204BTX IP Handbook*
- *UG0677: PolarFire FPGA Transceiver User Guide*
- *AD9371 Reference Link*
- *Identify ME User Guide*

2.2 Scope

This report describes the hardware setup used for interoperability testing and the test results of the JESD204B link. The following table lists the configurations of the tested device.

Table 1 • **Device Requirements**

Device	Link Rate (Gbps)	Link Width	JESD Version
AD9371 Transmitter	6.144	×2	JESD204B Subclass 1
AD9371 Receiver	6.144	×2	JESD204B Subclass 1

2.3 Software and Hardware Requirements

The following are the software and hardware requirements for interoperability tests.

Hardware Requirements:

- PolarFire Evaluation Kit
- ADRV9371-W/PCBZ Module
- Function Generator
- 110 V to 240 V AC to 12-V DC-Power Adapter
- USB A to Mini-B Cable
- SMA Cables

Software Requirements:

- Libero SoC v12.0
- Softconsole v6.0

Note: Please contact Microsemi Tech Support Team at *soc_tech@microsemi.com* for design files.

2.4 Interoperability Test Setup

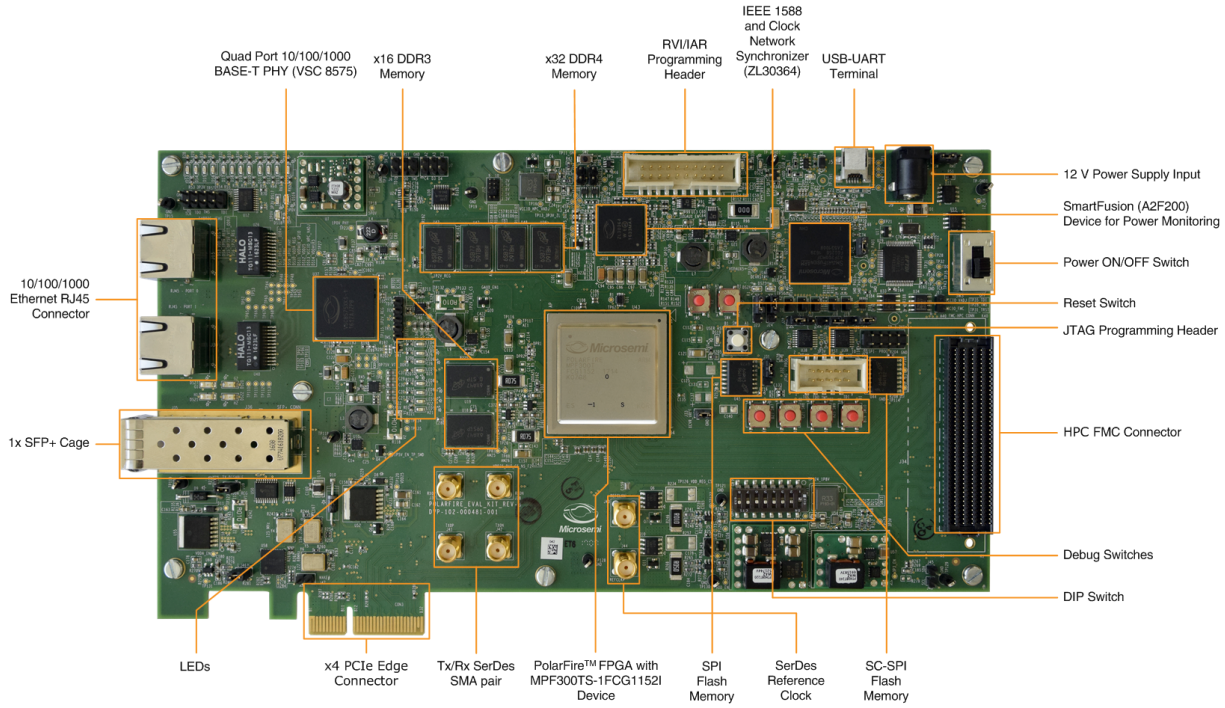
The interoperability test was performed on the PolarFire Evaluation Kit board with the MPF300TS-1FCG1152I device and the ADRV9371-W/PCBZ analog device module, as shown in the following figures.

ADRV9371-WPCBZ is a radio card designed to showcase AD9371, which is a high-performance wideband integrated RF transceiver intended for use in RF applications such as 4G base station, test and measurement applications, and software defined radios.
The ADRV9371-W/PCBZ analog device module operates over a wide tuning range of 300 MHz to 6 GHz. However, the RF performance is tempered by the wide band front end match. AD9371 is a highly integrated, wideband RF transceiver offering dual-channel transmitters and receivers, integrated synthesizers, and digital signal processing functions.The high-speed JESD204B interface supports lane rates of up to 6144 Mbps. Four lanes are dedicated to the transmitters and four lanes to the receiver and observation receiver channels.

The design for the interoperability test was developed using Libero SoC by instantiating the CoreJESD204BRX IP, CoreJESD204BTX IP, and other required IP cores in SmartDesign. The register configuration of AD9371 was done using a MiV soft processor instantiated in the design.

The following figure shows the hardware setup.

Figure 1 • **PolarFire Evaluation Kit**



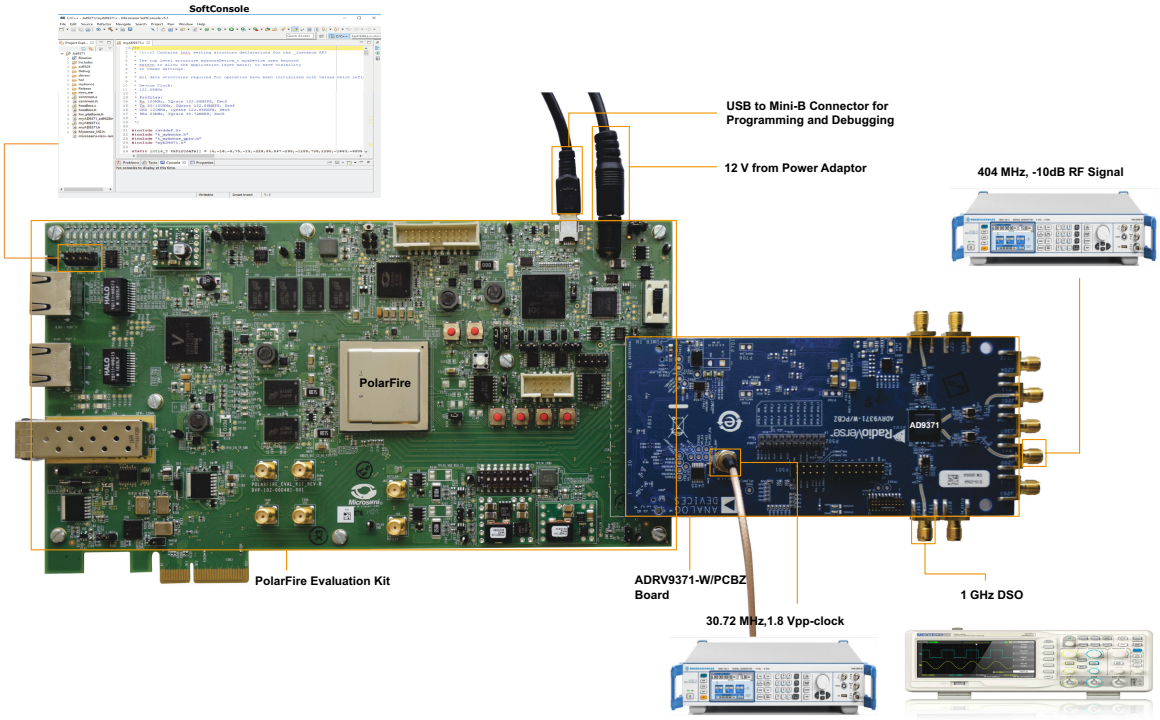
The ADRV9371-W/PCBZ evaluation module was used to evaluate the AD9371 transmitter and receiver. This module was connected to the HPC FMC connector of PolarFire Evaluation Kit.

30.72 MHz,1.8 Vpp reference clock was provided for AD9528, which is a low jitter clock generator.

Figure 2 • **ADRV9371-W/PCBZ Module**

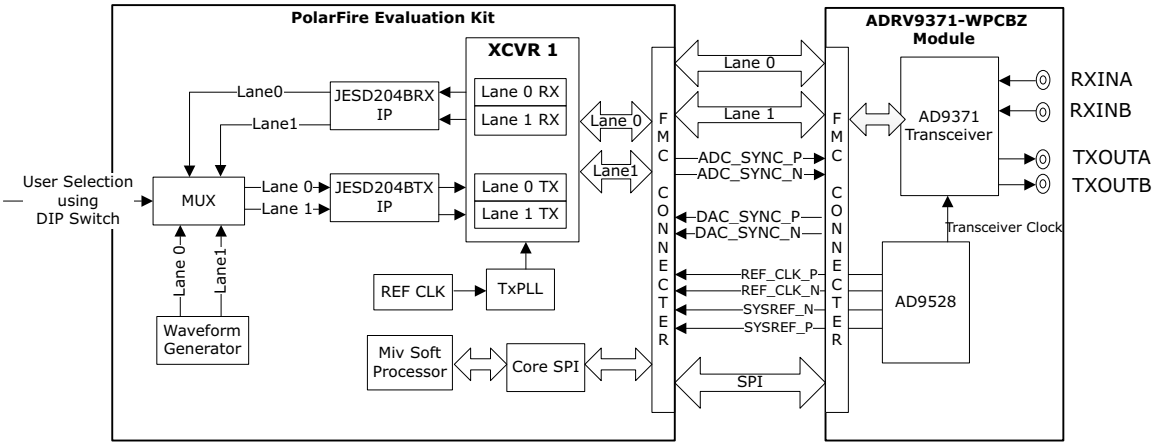
The following figure shows the hardware setup for interoperability tests.

Figure 3 • **Hardware Setup for Interoperability Tests with AD9371**



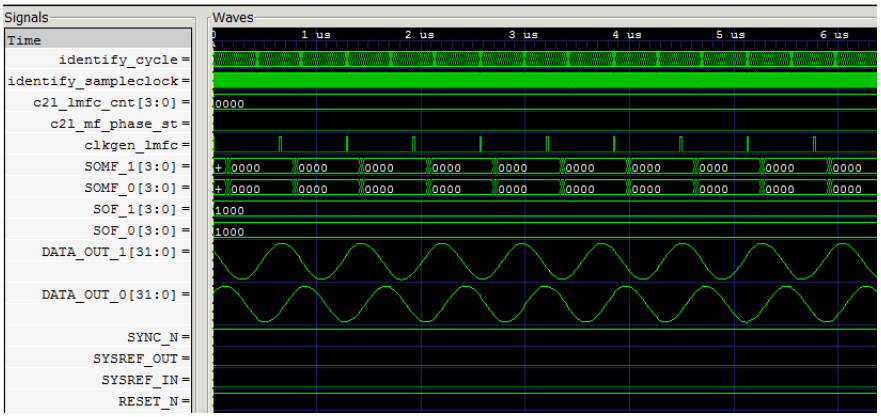
The following block diagram illustrates how signals flow in the hardware setup for interoperability tests.

Figure 4 • **Block Diagram of Interoperability Tests**



The following figure shows the data captured in Identify Debugger tool

Figure 5 • **Data Captured in Identify Debugger Tool**



2.5 Interoperability Test Settings

CoreJESD204BRX, CoreJESD204BTX, AD9371-Transmitter, and AD9371-Receiver were configured, as listed in the following table.

Table 2 • **CoreJESD204BRX, CoreJESD204BTX, AD9371-Transmitter, and AD9371-Receiver Configurations**

Parameter	Core JESD204BTX	Core JESD204BRX	AD9371-Transmitter	AD9371-Receiver	Description
SCR	0	0	0	0	Scramble enable/disable
L	2	2	2	2	Lanes
F	4	4	4	4	Octets per frame
K	32	32	32	32	Frames per multi-frame
M	4	4	4	4	Converters
CS	0	0	0	0	Control bits per sample
N	16	16	16	16	Sample resolution

Table 2 • **CoreJESD204BRX, CoreJESD204BTX, AD9371-Transmitter, and AD9371-Receiver Configurations**

Parameter	Core JESD204BTX	Core JESD204BRX	AD9371-Transmitter	AD9371-Receiver	Description
N'	16	16	16	16	Sample envelope
S	1	1	1	1	Samples per converter per frame
HD	0	0	0	0	High density mode
CF	0	0	0	0	Control bits per frame
SUBCLASSV	1	1	1	1	0×0/0×1

2.6 AD9371—Receiver Interoperability Tests

The following interoperability tests were performed on CoreJESD204BRX and AD9371-Receiver:

2.6.1 Test 1: Data Link Layer—Code Group Synchronization

On link startup, the receiver issues a synchronization request and the transmitter emits comma characters /K/ = /K28.5/. Identify Debugger was used to monitor the operation of the receiver data link layer.

The following table lists the data link layer—code group synchronization (CGS) test results.

Table 3 • **Data Link Layer—Code Group Synchronization Test Results**

Test Case	Objective	Description	Passing Criteria	Results
ADC1.1	Check if the receiver asserts SYNC_N signal when the link is down.	CoreJESD204BRX_0 -> SYNC_N signal is observed in Identify Debugger.	SYNC_N is low.	Passed.
ADC1.2	Check if SYNC_N request is de-asserted on receiving at least four successive /K/ characters.	CoreJESD204BRX_0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], and SYNC_N signals are observed in Identify Debugger.	K28.5 or /K/ character (0 × BC) is observed on DATA_OUT and SYNC_N is de-asserted on receiving at least four successive /K/ characters.	Passed.
ADC1.3	Check the full code group synchronization at receiver on receiving another four successive 8B/10B characters.	CoreJESD204BRX_0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], SYNC_N and CGS_ERR[3:0] signals are observed in Identify Debugger	CGS error is not asserted	Passed.

2.6.2 Test 2: Data Link Layer—Initial Lane Alignment Sequence

The following table lists the data link layer—initial lane alignment sequence (ILAS) test results.

Table 4 • **Data Link Layer—Initial Lane Alignment Sequence Test Results**

Test Case	Objective	Description	Passing Criteria	Results
ADC2.1	Check if the ILA phase starts after the CGS phase.	CoreJESD204BRX_0-> DATA_OUT_0[31:0], DATA_OUT_1[31:0], SOMF_0[3:0], SOMF_1[3:0], SOF_0[3:0], and SOF_1[3:0] signals are observed in Identify Debugger.	Multi-frame starts with 0×1C and is aligned to SOMF_0[3:0] and SOMF_1[3:0].	Passed.

Table 4 • **Data Link Layer—Initial Lane Alignment Sequence Test Results *(continued)***

Test Case	Objective	Description	Passing Criteria	Results
ADC2.2	Check the JESD configuration data in the second multi-frame	CoreJESD204BRX _0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], SOMF_0[3:0], SOMF_1[3:0], SOF_0[3:0], SOF_1[3:0], and LINK_CD_ERROR[3:0] signals are observed in Identify Debugger.	Observe the second multi-frame that starts with 0x1C followed by 0x9C and JESD204B configuration data.	Passed.

2.6.3 Test 3: Receiver Transport Layer

The following table lists the receiver transport layer test results.

Table 5 • **Receiver Transport Layer Test Results**

Test Case	Objective	Description	Passing Criteria	Results
ADC3.1	Check data integrity in test mode	ADC is configured in normal mode. CoreJESD204BRX _0 -> DATA_OUT_0[31:0], and DATA_OUT_1[31:0] signals are observed in Identify Debugger.	Received signal correlates with the input signal given for ADC sampling.	Passed.

2.6.4 Test 4: Descrambling

Scrambler is enabled in AD9371-ADC, and descrambler is enabled in CoreJESD204BRX IP. The following table lists the descrambling test results.

Table 6 • **Descrambling Test Results**

Test Case	Objective	Description	Passing Criteria	Results
ADC4.1	Check descrambler functionality.	ADC is configured in normal mode. CoreJESD204BRX _0 -> DATA_OUT_0[31:0], and DATA_OUT_1[31:0] signals are observed in Identify Debugger.	Received signal correlates with the input signal given for ADC sampling.	Passed.

2.6.5 Test 5: Deterministic Latency

The following table lists the JESD204B deterministic latency measurement test results.

Table 7 • **JESD204B Deterministic Latency Measurement Test Results – Subclass 1 Mode**

Test Case	Objective	Description	Passing Criteria	Results
ADC5.1	Check local multi-frame counter (LMFC) alignment	CoreJESD204BRX_0 -> clkgen_lmfc and SYSREF_IN signals are observed in Identify Debugger.	SYSREF_IN is aligned to clkgen_lmfc.	Passed.

Table 7 • **JESD204B Deterministic Latency Measurement Test Results – Subclass 1 Mode *(continued)***

Test Case	Objective	Description	Passing Criteria	Results
ADC5.2	SYSREF capture	CoreJESD204BRX _0 -> c2_mf_phase and SYSREF_IN signals are observed in Identify Debugger.	LMFC counter restarts after the SYSREF_IN capture.	Passed.
ADC5.3	Check latency from start de-assertion of SYNC_N to first user data output.	Check if latency is fixed for every link reset/initialization.	Latency must be same for link reset/initialization even if the reset is performed multiple times.	Passed.
ADC5.4	Check the data latency during user data phase.	Check if the data latency is fixed during the user data phase. CoreJESD204BRX_0 -> DATA_OUT_0[31:0], and DATA_OUT_1[31:0] signals are observed in Identify Debugger.	The user data is seen without distortion.	Passed.
ADC5.5	Check the data latency during user data phase.	Transmit a pulse from pulse generator block and loop it back on Rx and Tx on hardware.	Latency must be same for link reset/initialization even if the reset is performed multiple times.	Passed.

2.7 AD9371-Transmitter Interoperability Tests

The following interoperability tests were performed on CoreJESD204BTX:

- Test 1: Data Link Layer—Code Group Synchronization, page 9
- Test 2: Data Link Layer—Initial Lane Alignment Sequence, page 10
- Test 3: Transmitter Transport Layer, page 10
- Test 4: Descrambling, page 11
- Test 5: Deterministic Latency, page 11

2.7.1 Test 1: Data Link Layer—Code Group Synchronization

On link startup, the receiver issues a synchronization request and the transmitter emits comma characters /K/ = /K28.5/. Identify Debugger was used to monitor the operation of the receiver data link layer. The following table lists the data link layer—code group synchronization (CGS) test results.

Table 8 • **Data Link Layer—Code Group Synchronization**

Test Case	Objective	Description	Passing Criteria	Results
DAC1.1	Check if the receiver asserts SYNC_N signal when the link is down.	CoreJESD204BTX _0 -> SYNC_request signal is observed in Identify Debugger.	SYNC_request goes low.	Passed.
DAC1.2	Check if at least four successive /K/ characters are transmitted on SYNC_N assertion.	CoreJESD204BTX _0 -> TX_DATA _0 [31:0], TX_DATA _1 [31:0], and SYNC_N signals are observed in Identify Debugger.	At least four K28.5 or /K/ characters are observed on TX_DATA _0 [31:0], TX_DATA _1 [31:0], on assertion of SYNC_N.	Passed.

Table 8 • **Data Link Layer—Code Group Synchronization *(continued)***

Test Case	Objective	Description	Passing Criteria	Results
DAC1.3	Check full code group synchronization at the transmitter after the correct transmission of another four 8B/10B characters.	CoreJESD204BTX _0 ->TX_STATE[1:0] signal is observed in Identify Debugger.	CoreJESD204BTX -> TX_STATE changes from SYNC_ST(0x00) to INIT_LANE_ST (0x01).	Passed.

2.7.2 Test 2: Data Link Layer—Initial Lane Alignment Sequence

The following table lists the data link layer—initial lane alignment sequence (ILAS) test results.

Table 9 • **Data Link Layer—Initial Lane Alignment Sequence**

Test Case	Objective	Description	Passing Criteria	Results
DAC2.1	Check if the ILAS phase starts after the CGS phase	– CoreJESD204BTX _0 -> TX_DATA _0 [31:0], and TX_DATA _1 [31:0] signals are observed in Identify Debugger. – Check de-framer status register.	– Observe the /R/, /A/, and /Q/ in the correct order of ILAS. – De-framer status register is 0x68	Passed.
DAC2.2	Check the JESD configuration data	Check if the DAC receives the expected configuration data.	Check if the DAC link configuration data matches with the CoreJESD204BTX link configuration data.	Passed.
DAC2.3	Check if the ILA phase is completed successfully	– CoreJESD204BTX _0 -> TX_STATE[1:0] signal is observed in Identify Debugger. – Check de-framer status register.	– CoreJESD204BTX TX_STATE changes from INIT_LANE_ST (0x01) to DATA_ENC_ST (0x02). – De-framer status register is 0x68.	Passed.

2.7.3 Test 3: Transmitter Transport Layer

The following table lists the transmitter transport layer test results.

Table 10 • **Receiver Transport Layer**

Test Case	Objective	Description	Passing Criteria	Results
DAC3.1	Check the data phase	Check if the expected waveform is obtained in DAC outputs.	Signal monitored at AD9371 transmitter, correlates with the analog sine wave input given to AD9371 Receiver	Passed.
DAC3.2	Check the data rate	CoreJESD204BTX transfer data at 6144 Mbps per lane for LMF = 244.	Signal monitored at AD9371 Transmitter, correlates with the analog sine wave input given to AD9371 Receiver.	Passed.

2.7.4 Test 4: Descrambling

Scrambler is enabled in CoreJESD204BTX IP, and descrambler is enabled in AD9371-DAC. The following table lists the descrambling test results.

Table 11 • **Descrambling Test Results**

Test Case	Objective	Description	Passing Criteria	Results
DAC4.1	Check the scrambler functionality	Enable scrambler and check data at the output.	Signal monitored at AD9371 transmitter, correlates with the analog sine wave input given to AD9371 Receiver	Passed.

2.7.5 Test 5: Deterministic Latency

The following table lists the JESD204B deterministic latency measurement test results.

Table 12 • **Deterministic Latency**

Test Case	Objective	Description	Passing Criteria	Results
DAC5.1	Check the LMFC alignment.	CoreJESD204BTX _0 -> clkgen_lmfc and SYSREF_OUT signals are observed in Identify Debugger.	SYSREF_OUT must be aligned with clkgen_lmfc	Passed.
DAC5.2	SYSREF capture	CoreJESD204BTX _0 -> c2l_mf_phase and SYSREF_OUT signals are observed in Identify Debugger.	LMFC counter restarts after the SYSREF_OUT capture.	Passed.
DAC5.3	Check the data latency during user data phase.	Check if the data latency is fixed during the user data phase. CoreJESD204BTX_0 -> TX_DATA _0 [31:0], and TX_DATA _1 [31:0] signals are observed in Identify Debugger.	Latency must be same for link reset/initialization even if the reset is performed multiple times.	Passed.
DAC5.4	Check the data latency during user data phase.	Transmit a pulse from pulse generator block and loop it back on Rx and Tx on hardware.	Latency must be same for link reset/initialization even if the reset is performed multiple times.	Passed.