TR0035
Test Report
PolarFire FPGA CoreJESD204BRX and CoreJESD204BTX Interoperability for AD9680 and AD9144

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document.

2 PolarFire FPGA CoreJESD204BRX and CoreJESD204BTX Interoperability Test Report

Microsemi provides interfacing solutions for analog-to-digital converter (ADC) and digital-to-analog converter (DAC) devices using the JESD204B JEDEC standards. These solutions are provided as DirectCore soft IPs (CoreJESD204BRX and CoreJESD204BTX) in Libero® SoC PolarFire®. These IP cores interface with transceivers of PolarFire FPGA devices. This report provides the results of interoperability tests performed on a third-party ADC and DAC device. The interoperability test results describe the JESD204B link parameters, hardware test setup, equipment used, and final test report of Microsemi DirectCores: CoreJESD204BRX and CoreJESD204BTX.

2.1 References

- *CoreJESD204BRX IP Handbook*
- *CoreJESD204BTX IP Handbook*
- *UG0677: PolarFire FPGA Transceiver User Guide*
- *AD-FMCDAQ2-EBZ User Guide*
- *Identify ME User Guide*

2.2 Scope

This report describes the hardware setup used for interoperability testing and the test results of the JESD204B link. The following table lists the configuration of the tested device.

Table 1 • **Device Requirements**

Device	Link Rate (Gbps)	Link Width	Subclass
AD9680 ADC	6.25 Gbps	×4	0,1
AD9144 DAC	6.25 Gbps	×4	0,1

2.3 Software and Hardware Requirements

The following are the hardware and software requirements for interoperability tests.

Hardware Requirements:

- PolarFire Evaluation Kit
- AD-FMCDAQ2-EBZ module
- Function Generator
- 110 V to 240 V AC to 12-V DC-Power Adapter
- USB A to Mini-B Cable

Software Requirements:

- Libero SoC PolarFire
- Configurator GUI

Note: For design files, contact Microsemi Tech Support Team at *soc_tech@microsemi.com*.

2.4 Interoperability Test Setup

The interoperability test is performed on the PolarFire Evaluation Kit board with the MPF300TS-1FCG1152I device as shown in the following figure and the AD-FMCDAQ2-EBZ analog device module, as shown in the Figure 2, page 4.

This evaluation module is used to evaluate the AD9680 (ADC) and AD9144 (DAC). The AD9680 is a dual, 14-bit, 1.25 GSPS/1 GSPS/820 MSPS/ 500 MSPS ADC. The device has an on-chip buffer and sample-and-hold circuit designed for low power, small size, and ease of use. This device is designed for sampling wide bandwidth analog signals of up to 2 GHz.The AD9144 is a quad, 16-bit, high dynamic range DAC that provides a maximum sample rate of 2.8 GSPS, permitting a multi-carrier generation up to the Nyquist frequency.

The design for the test is developed using the Libero SoC PolarFire software by instantiating the CoreJESD204BRX IP, CoreJESD204BTX IP and other required IP cores in SmartDesign. Microsemi's Configurator GUI is used to configure the registers of AD9680, AD9144 and AD9523.

The following figure shows the hardware setup.

Figure 1 • **PolarFire Evaluation Kit**

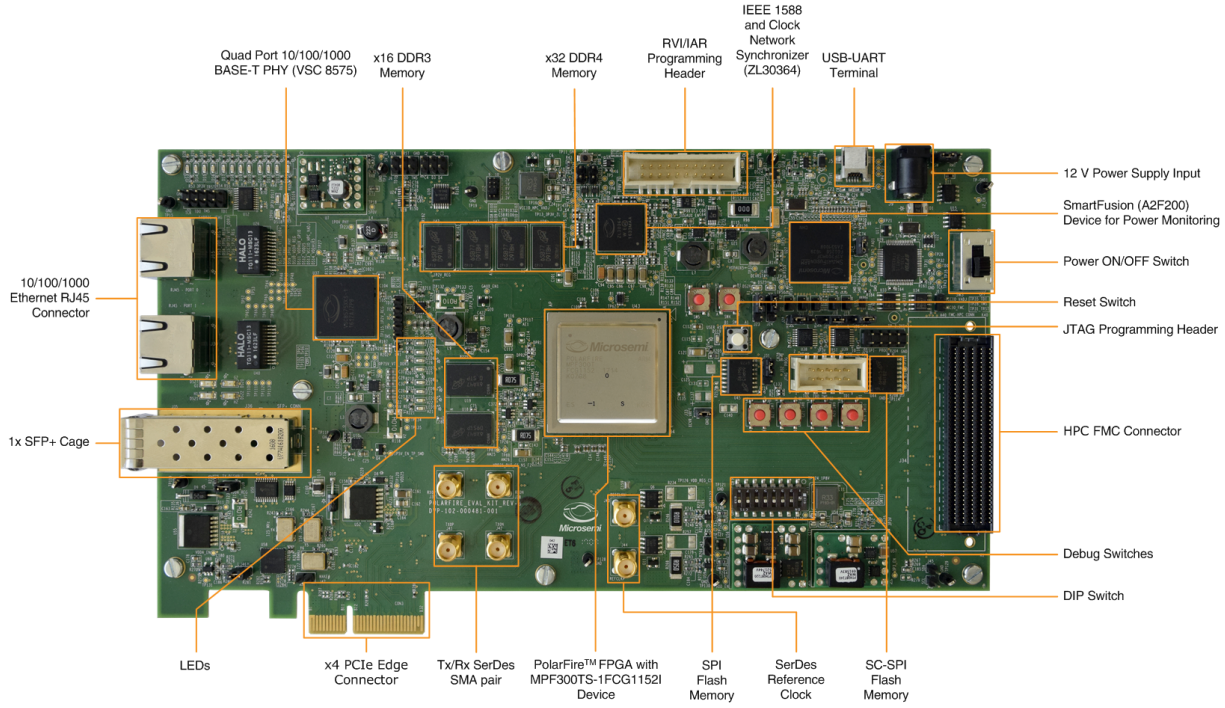
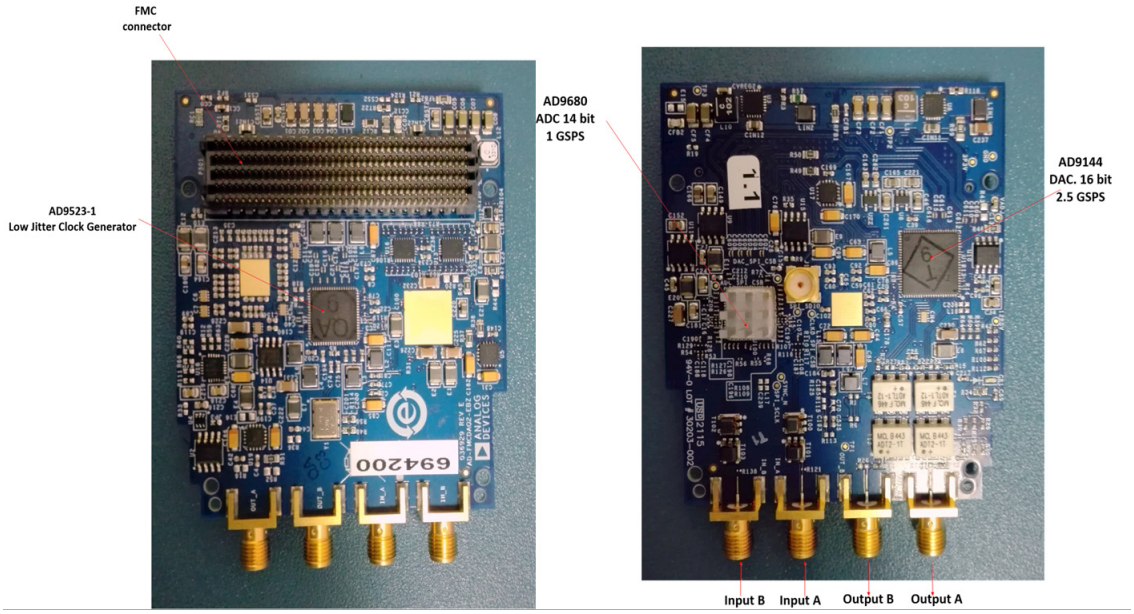
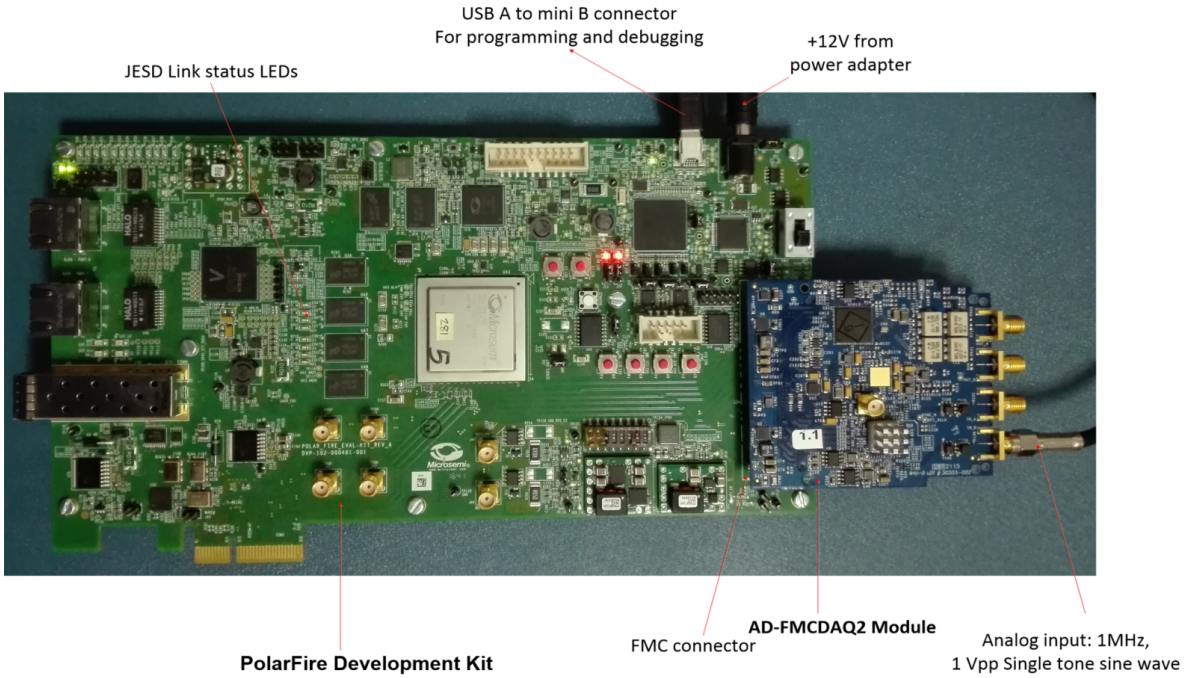


Figure 2 • **AD-FMCDAQ2-EBZ Module**



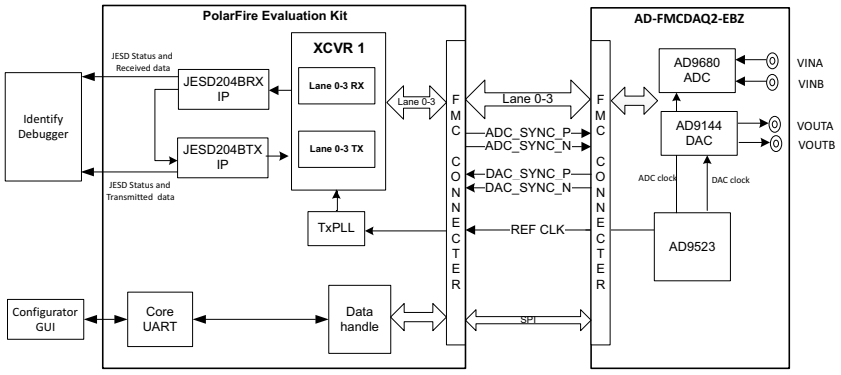
The AD-FMCDAQ2 evaluation module is used to evaluate the AD9680-ADC and AD9144-DAC.This module is connected to the FMC HPC connector of PolarFire Evaluation Kit. 1Mhz,1-Vpp single tone sine wave is fed to the analog input channel. The following figure shows the hardware setup for Interoperability test. The AD9523 module provides a low power, multi-output, clock distribution function with low jitter performance, along with an on-chip phase-locked loop (PLL) and voltage-controlled oscillator (VCO).

Figure 3 • **Hardware Setup for Interoperability Tests with AD9680 and AD9144**



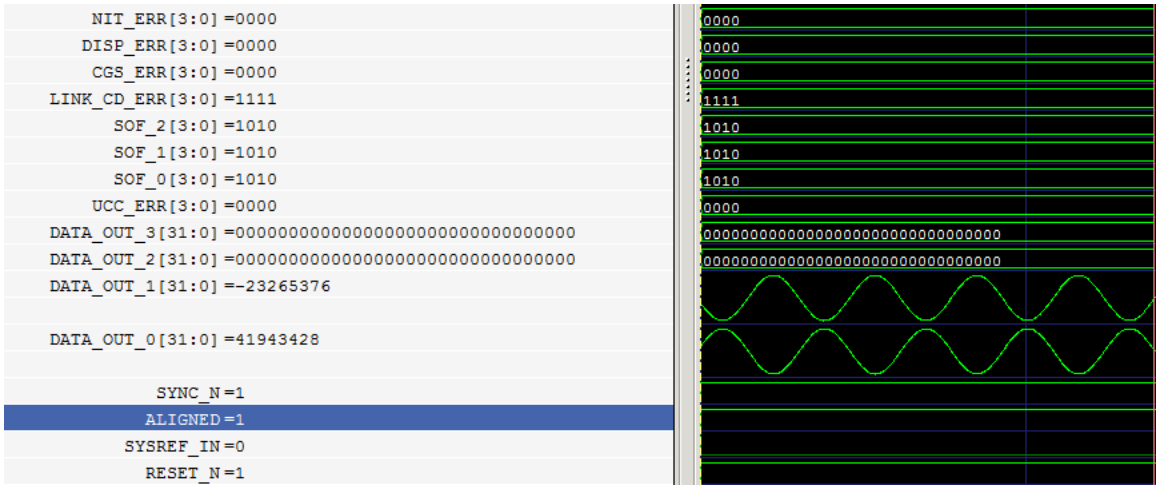
The following block diagram illustrates how signals flow in the hardware setup for interoperability tests.

Figure 4 • **Block Diagram of Interoperability Tests**



The following figure shows the data received from AD9680 in Identify Debugger tool.

Figure 5 • **Data Captured in Identify Debugger Tool**



2.5 Interoperability Test Settings

CoreJESD204BRX, CoreJESD204BTX, AD9680-ADC, and AD9144-DAC are configured, as shown in the following table.

Table 2 • **CoreJESD204BRX, CoreJESD204BTX, AD9680-ADC and AD9144-DAC Configurations**

Parameter	Core JESD204BTX	Core JESD204BRX	AD9680-ADC	AD9144-DAC	Description
SCR	0	0	0	0	Scramble enable/disable
L	4	4	4	4	Lanes
F	2	2	2	2	Octets per frame
K	32	32	32	32	Frames per multi-frame
M	2	2	2	2	Converters
CS	0	0	0	0	Control bits per sample
N	16	16	16	16	Sample resolution
N'	16	16	16	16	Sample envelope

Table 2 • **CoreJESD204BRX, CoreJESD204BTX, AD9680-ADC and AD9144-DAC Configurations**

Parameter	Core JESD204BTX	Core JESD204BRX	AD9680-ADC	AD9144-DAC	Description
S	2	2	2	2	Samples per converter per frame
HD	0	0	0	0	High density mode
CF	0	0	0	0	Control bits per frame
SUBCLASSV	0	0	0	0	0×0/0×1

2.6 ADC-AD9680 Interoperability Tests

The following interoperability tests were performed on **CoreJESD204BRX** and **ADC-AD9680**:

2.6.1 Test 1: Data Link Layer—Code Group Synchronization

On link startup, the receiver issues a synchronization request and the transmitter emits comma characters /K/ = /K28.5/. Identify Debugger is used to monitor the operation of the receiver data link layer. The following table lists the data link layer - code group synchronization (CGS) test results.

Table 3 • **Data Link Layer—Code Group Synchronization Test Results**

Test Case	Objective	Description	Passing Criteria	Results
ADC1.1	Check if the receiver asserts SYNC_N signal when the link is down.	CoreJESD204BRX_0 -> SYNC_N signal is observed in Identify Debugger.	SYNC_N is low.	Passed.
ADC1.2	Check if SYNC_N request is de-asserted on receiving at least four successive /K/ characters.	CoreJESD204BRX_0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0], and SYNC_N signals are observed in Identify Debugger.	K28.5 or /K/ character (0 × BC) is observed on DATA_OUT and SYNC_N is de-asserted on receiving at least four successive /K/ characters.	Passed.
ADC1.3	Check the full code group synchronization at receiver on receiving another four successive 8B/10B characters.	CoreJESD204BRX_0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0], SYNC_N and CGS_ERR[3:0] signals are observed in Identify Debugger	CGS error is not asserted	Passed.

2.6.2 Test 2: Data Link Layer—Initial Lane Alignment Sequence

The following table lists the data link layer—initial lane alignment sequence (ILAS) test results.

Table 4 • **Data Link Layer—Initial Lane Alignment Sequence Test Results**

Test Case	Objective	Description	Passing Criteria	Results
ADC2.1	Check if the ILA phase starts after the CGS phase.	CoreJESD204BRX_0-> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0], SOMF_0[3:0], SOMF_1[3:0], SOMF_2[3:0], SOMF_3[3:0], SOF_0[3:0], SOF_1[3:0], SOF_2[3:0], SOF_3[3:0], signals are observed in Identify Debugger.	Multi-frame starts with 0×1C and is aligned to SOMF_0[3:0], SOMF_1[3:0], SOMF_2[3:0], SOMF_3[3:0],	Passed.
ADC2.2	Check the JESD configuration data in the second multi-frame	CoreJESD204BRX _0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0], SOMF_0[3:0], SOMF_1[3:0], SOMF_2[3:0], SOMF_3[3:0], SOF_0[3:0], SOF_1[3:0], SOF_2[3:0], SOF_3[3:0], and LINK_CD_ERROR[3:0] signals are observed in Identify Debugger.	Observe the second multi-frame that starts with 0x1C followed by 0x9C and JESD204B configuration data.	Passed.

2.6.3 Test 3: Receiver Transport Layer

The following table lists the receiver transport layer test results.

Table 5 • **Receiver Transport Layer Test Results**

Test Case	Objective	Description	Passing Criteria	Results
ADC3.1	Check data integrity in test mode	ADC is configured in long transport layer test pattern mode. CoreJESD204BRX _0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0], signals are observed in Identify Debugger.	Received signal correlates with the transport layer test pattern.	Passed.

Table 5 • **Receiver Transport Layer Test Results *(continued)***

Test Case	Objective	Description	Passing Criteria	Results
ADC3.2	Check data integrity in normal mode	ADC is configured in normal mode. CoreJESD204BRX _0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0]. signals are observed in Identify Debugger.	Received signal (monitored in identify tool) correlates with the analog sine wave input given for ADC sampling.	Passed.

2.6.4 Test 4: Descrambling

Scrambler is enabled in ADC, and descrambler is enabled in CoreJESD204BRX IP. The following table lists the descrambling test results.

Table 6 • **Descrambling Test Results**

Test Case	Objective	Description	Passing Criteria	Results
ADC4.1	Check descrambler functionality.	ADC is configured in in normal mode. CoreJESD204BRX _0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0]. signals are observed in Identify Debugger.	Received signal (monitored in identify tool) correlates with the analog sine wave input given for ADC sampling.	Passed.

2.6.5 Test 5: Deterministic Latency

CoreJESD204BRX IP and ADC are configured in **Subclass 1** mode. The following table lists the JESD204B deterministic latency measurement test results.

Table 7 • **JESD204B Deterministic Latency Measurement Test Results – Subclass 1 Mode**

Test Case	Objective	Description	Passing Criteria	Results
ADC5.1	Check local multi-frame counter (LMFC) alignment	CoreJESD204BRX_0 -> clkgen_lmfc and SYSREF_IN signals are observed in Identify Debugger.	SYSREF_IN is aligned to clkgen_lmfc.	Passed.
ADC5.2	SYSREF capture	CoreJESD204BRX _0 -> c2l_mf_phase, and SYSREF_IN signals are observed in Identify Debugger.	LMFC counter restarts after the SYSREF_IN capture.	Passed.
ADC5.3	Check latency from start de-assertion of SYNC_N to first user data output.	Check if latency is fixed for every link reset/initialization.	Latency must be same for link reset/initialization	Passed.

Table 7 • **JESD204B Deterministic Latency Measurement Test Results – Subclass 1 Mode *(continued)***

Test Case	Objective	Description	Passing Criteria	Results
ADC5.4	Check the data latency during user data phase.	Check if the data latency is fixed during the user data phase. CoreJESD204BRX_0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0]. signals are observed in Identify Debugger.	The ramp pattern without distortion.	Passed.

2.7 DAC- AD9144 Interoperability Tests

The following interoperability tests are performed on **CoreJESD204BTX IP** and **DAC-AD9144**:

2.7.1 Test 1: Data Link Layer—Code Group Synchronization

On link startup, the receiver issues a synchronization request and the transmitter emits comma characters /K/ = /K28.5/. Identify Debugger is used to monitor the operation of the receiver data link layer.

The following table lists the data link layer—CGS test results.

Table 8 • **Data Link Layer—Code Group Synchronization**

Test Case	Objective	Description	Passing Criteria	Results
DAC1.1	Check if the receiver asserts SYNC_N signal when the link is down.	CoreJESD204BTX _0 -> SYNC_request signal is observed in Identify Debugger.	SYNC_request goes low.	Passed.
DAC1.2	Check if at least four successive /K/ characters are transmitted on SYNC_N assertion.	CoreJESD204BTX _0 -> TX_DATA _0 [31:0], TX_DATA _1 [31:0], TX_DATA _2 [31:0], TX_DATA _3 [31:0] and SYNC_N signals are observed in Identify Debugger.	At least four K28.5 or /K/ characters are observed on TX_DATA _0[31:0], TX_DATA_1[31:0], TX_DATA_2[31:0], TX_DATA_3[31:0]. on assertion of SYNC_N.	Passed.
DAC1.3	Check full code group synchronization at the transmitter after the correct transmission of another four 8B/10B characters.	CoreJESD204BTX _0 ->TX_STATE[1:0] signal is observed in Identify Debugger.	CoreJESD204BTX -> TX_STATE changes from SYNC_ST(0x00) to INIT_LANE_ST (0x01).	Passed.

2.7.2 Test 2: Data Link Layer—Initial Lane Alignment Sequence

The following table lists the data link layer—ILAS test results.

Table 9 • **Data Link Layer—Initial Lane Alignment Sequence**

Test Case	Objective	Description	Passing Criteria	Results
DAC2.1	Check if the ILAS phase starts after the CGS phase	– CoreJESD204BTX _0 -> TX_DATA_0[31:0], TX_DATA_1[31:0], TX_DATA_2[31:0], TX_DATA_3[31:0]. signals are observed in Identify Debugger.	– Observe the /R/, /A/, and /Q/ in the correct order as per ILAS. – The flags /R/, /A/, /Q/ and /K/ are set in DAC K28 registers.	Passed.
DAC2.2	Check the JESD configuration data	Check if the DAC receives the expected configuration data.	DAC link configuration data matches with the CoreJESD204BTX link configuration data.	Passed.
DAC2.3	Check if the ILA phase is completed successfully	– CoreJESD204BTX _0 -> TX_STATE[1:0] signal is observed in Identify Debugger.	– CoreJESD204BTX TX_STATE changes from INIT_LANE_ST (0x01) to DATA_ENC_ST (0x02).	Passed.

2.7.3 Test 3: Receiver Transport Layer

The following table lists the receiver transport layer test results.

Table 10 • **Receiver Transport Layer**

Test Case	Objective	Description	Passing Criteria	Results
DAC3.1	Check the data phase	Check if the expected waveform is obtained in DAC outputs.	Waveform on the scope at DAC-AD9144 output correlates to the ADC-AD9680 sine wave input.	Passed.
DAC3.2	Check the data rate	CoreJESD204BTX transfer data at 6.25 Gbps per lane for LMF = 422.	Waveform on the scope at DAC-AD9144 output correlates to the ADC-AD9680 sine wave input.	Passed.

2.7.4 Test 4: Descrambling

Scrambler is enabled in DAC and descrambler is enabled in CoreJESD204BTX IP. The following table lists the descrambling test results.

Table 11 • **Descrambling Test Results**

Test Case	Objective	Description	Passing Criteria	Results
DAC4.1	Check the scrambler functionality	Enable scrambler and check data at the output.	Waveform on the scope at DAC-AD9144 output correlates to the ADC-AD9680 sine wave input.	Passed.

2.7.5 Test 5: Deterministic Latency

Subclass 1 Mode

CoreJESD204BTX IP and DAC are configured in **Subclass 1** mode. The following table lists the JESD204B deterministic latency measurement test results.

Table 12 • **Deterministic Latency**

Test Case	Objective	Description	Passing Criteria	Results
DAC5.1	Check the LMFC alignment.	CoreJESD204BTX _0 -> clkgen_lmfc and SYSREF_IN signals are observed in Identify Debugger.	SYSREF_IN is aligned with clkgen_lmfc	Passed.
DAC5.2	SYSREF capture	CoreJESD204BTX _0 -> c2l_mf_phase and SYSREF_IN signals are observed in Identify Debugger.	LMFC counter restarts after the SYSREF_IN capture.	Passed.
DAC5.3	Check the data latency during user data phase.	Check if the data latency is fixed during the user data phase. CoreJESD204BTX_0 -> TX_DATA_0[31:0], TX_DATA_1[31:0], TX_DATA_2[31:0], TX_DATA_3[31:0], signals are observed in Identify Debugger.	Latency must be same for link reset/initialization.	Passed.