White Paper

Chip-Scale Atomic Clock (CSAC) Performance During Rapid Temperature Change

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The chip-scale atomic clock (CSAC) is the world's lowest-power, lowest-profile atomic clock. Its unique 1PPS input eases the design process by allowing an external reference to quickly calibrate the device. Thousands of units are deployed every year in a variety of applications, from seismic sensors on the bottom of the ocean to the space CSAC aboard low-earth-orbit satellites.

For mobile applications, frequency and timing stability in variable temperature environments is critical. Choosing the best oscillator for the job can be confusing when comparing product specifications from different manufacturers, or even different product lines within the same company. The reason is that commercial oscillators are not held to any standard test, so the temperature profile (temperature range, ramp rate, and number of cycles) used can vary from product to product.

Atomic clocks and oscillators are generally considered to have superior temperature stability over their crystal-based counterparts. This is mainly due to the sealed (Cesium or Rubidium) gas cell's isolation from the outside environment. There are other factors that also contribute to an atomic oscillators' temperature resistance, as discussed later.

This paper will compare CSAC performance to that of an OCXO with a similar stability-versus-temperature specification. The paper will also discuss how time, temperature, and initial frequency errors can effect holdover timing error. For the purposes of this paper, holdover means the period of time when an oscillator is allowed to free-run. The frequency and timing error that accumulates during holdover is relative to a perfect timing reference.

The results of this analysis will show that a CSAC and an OCXO with similar specifications do not necessarily have the same performance—the CSAC is superior when subjected to a rapid ambient temperature change.

Effects on Timing Error: Elapsed Time

With a 9 x 10^{-10}/mo Hz/Hz typical aging rate, the CSAC has pretty good frequency drift (and corresponding time error). Its performance is similar to the best performing OCXOs. Time error can be calculated from published aging rates, as shown in References (see page 8). Taking the result of their derivation, the timing error accumulation over time is given as follows:

Equation 1

$$E(t) = E_0 + \left(y_0 t + \frac{1}{2}at^2\right) + \int_0^t E_i(t)dt + \varepsilon(t)$$

where,

$E(t)$: Time error accumulation at time t after initial synchronization
a: Clock frequency drift (or aging) rate
E_0: Initial time error at $t = 0$
$E_i(t)$: Fractional frequency offset due to environmental effects (such as temperature)
y_0: Initial fractional frequency at t = 0
$\varepsilon(t)$: Error due to random fractional frequency fluctuations

For simplification purposes, we have assumed zero initial phase or frequency offset and zero environmental perturbation, which reduces the equation to the following:

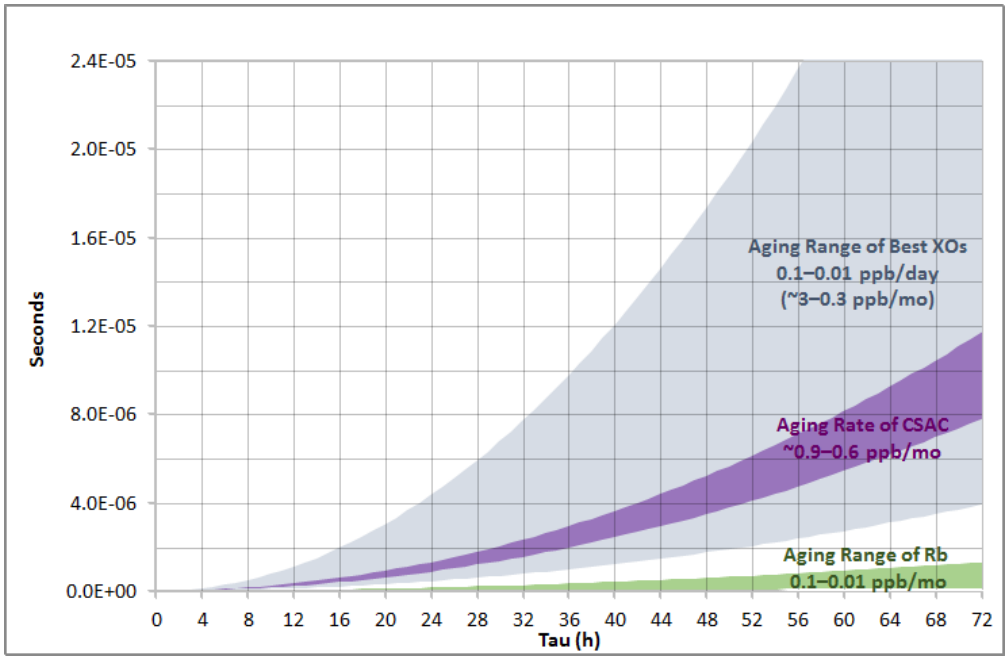
Equation 2

$$E(t) = \frac{1}{2}at^2$$

The following graph and table show predicted time error over 72 hours of the CSAC, high-performance OCXOs, and Rubidium atomic oscillators. CSAC will accumulate ~1 µs in 24 hours, ~5 µs in 48 hours, and 8 µs to 12 µs in 72 hours. These calculations were made based on typical observed aging rates of 0.6 ppb /mo to 0.9 ppb/mo.

Note: Throughout this document, RF output (10 MHz) performance of the CSAC will be shown. The CSAC 1PPS output is directly derived from the RF output, so it should be expected that the 1PPS would behave in a similar manner.

Time Error Derived from Aging Rates (at constant 25 °C)



Oscillator vs. Time Error

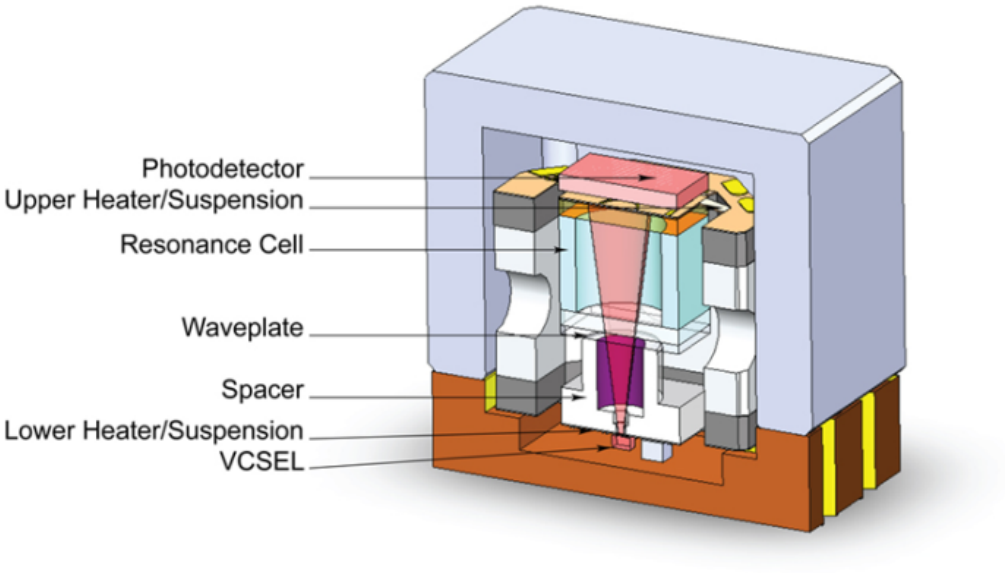
Oscillator	24 Hours	48 Hours	72 Hours
OCXO	0.3 µs to 4.5 µs	1.9 µs to 17 µs	4 µs to 28 µs
CSAC	0.5 µs to 1 µs	3.5 µs to 5 µs	8 µs to 12 µs
Rubidium	<0.2 µs	<0.5 µs	0.5 µs to 1.5 µs

Effects on Timing Error: Temperature

The previous calculation is not practical for mobile applications where the oscillator is exposed to temperature variations. Timing error due to those effects cannot be calculated by simply looking at a datasheet temperature specification (commonly referred to as temperature coefficient). Ramp rate, dwell time, airflow, number of cycles, and so on will all effect the outcome. The oscillator design and sample data must be considered to choose the best performer.

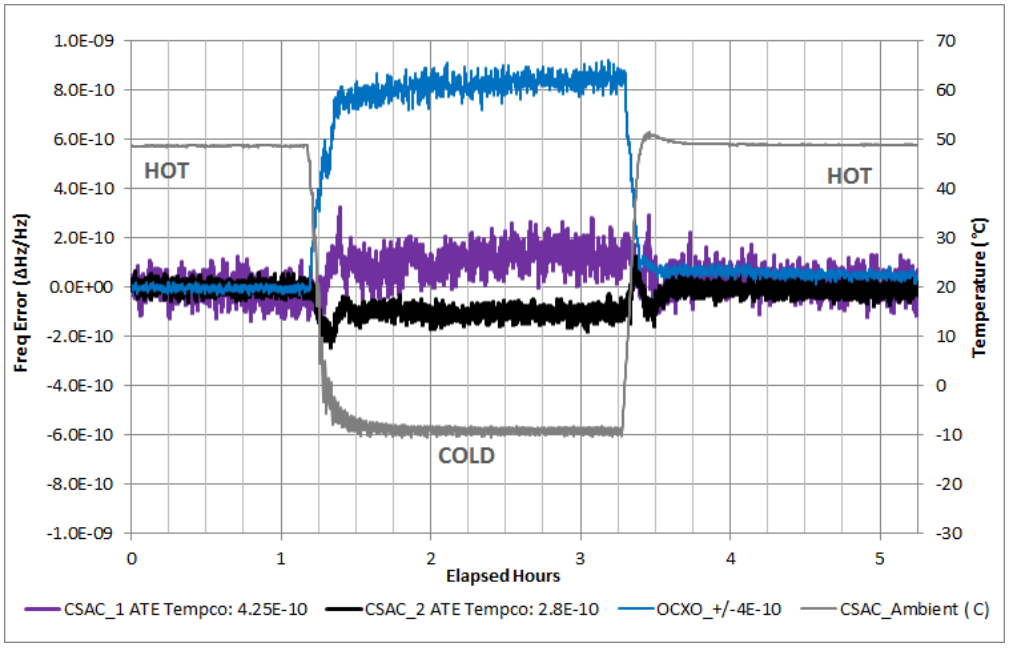
The CSAC design, shown in the following illustration, is unique in that the physics (laser, resonance cell, and photodetector) is vacuum-packaged to eliminate convection/conduction effects, with an overall thermal resistance of 7000 °C/W. Its tensioned, polyimide suspension further isolates the physics from outside vibration or thermal-induced mechanical stresses.

CSAC Physics Package



Thanks to the design of the CSAC, the temperature ramp-rate of its environment has little impact on its frequency response. The following two graphs show an example of an aggressive temperature profile. The oscillators are soaked at a hot temperature (50 °C) for over 1 hour before being rapidly cooled to –10 °C in about 12 minutes (5 °C/min). They are soaked at the cold temperature for 2 hours before they are rapidly returned to the hot temperature.

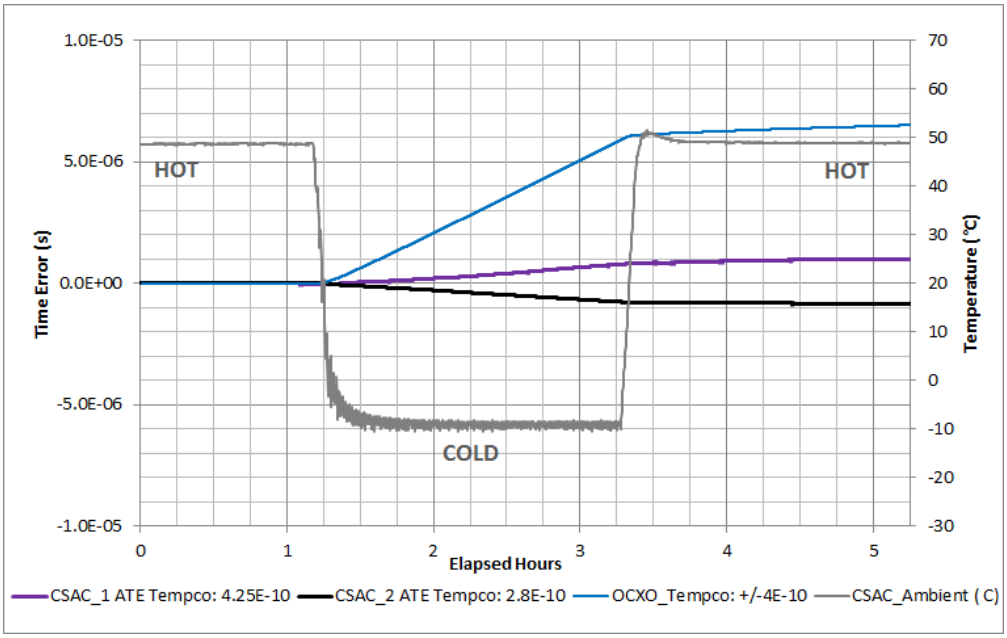
Frequency Response when Exposed to –10 °C to 50 °C Temperature Profile



Both CSACs, as shown by the purple and black traces, varied <±3 x 10^{-10} Hz/Hz. For comparison, an OCXO with similar specified temperature coefficient was subjected to the same test. Its frequency response was 3x–4x worse.

Note: The CSAC temperature coefficient specification is ±5 x 10^{-10} from –10 °C to 70 °C. OCXO is specified as ±4 x 10^{-10} from 0 °C to 70 °C. Measured factory temperature coefficient for CSAC_1 and CSAC_2 was 4.25 x 10^{-10} and 2.8 x 10^{-10}, respectively.

Phase Response when Exposed to –10 °C to 50 °C Temperature Profile



The following table lists the corresponding time error. At ~1 µs of time error, the CSACs are clearly superior when compared to a commercial OCXO, which accumulated 6.5 µs. A CSAC's thermal response approaches the performance of larger, more power-hungry Rubidium-based atomic oscillators.

Oscillator vs. Time Error

Oscillator	2 Hours	3 Hours	5 Hours
OCXO	2 µs	5 µs	6.5 µs
CSAC 1	0.1 µs	0.7 µs	1.1 µs
CSAC 2	–0.2 µs	–0.8 µs	–0.9 µs

Looking back at equation 1, we have demonstrated performance assuming zero initial phase and frequency offset. This time, however, the environmental effects are non-zero.

Equation 3

$$E(t) = \frac{1}{2}at^2 \int_0^t E_i(t)dt + \varepsilon(t)$$

Effects on Timing Error: Initial Frequency Offset

The temperature response of atomic oscillators is relatively small, so any initial frequency offset could have a comparatively larger impact on holdover timing errors.

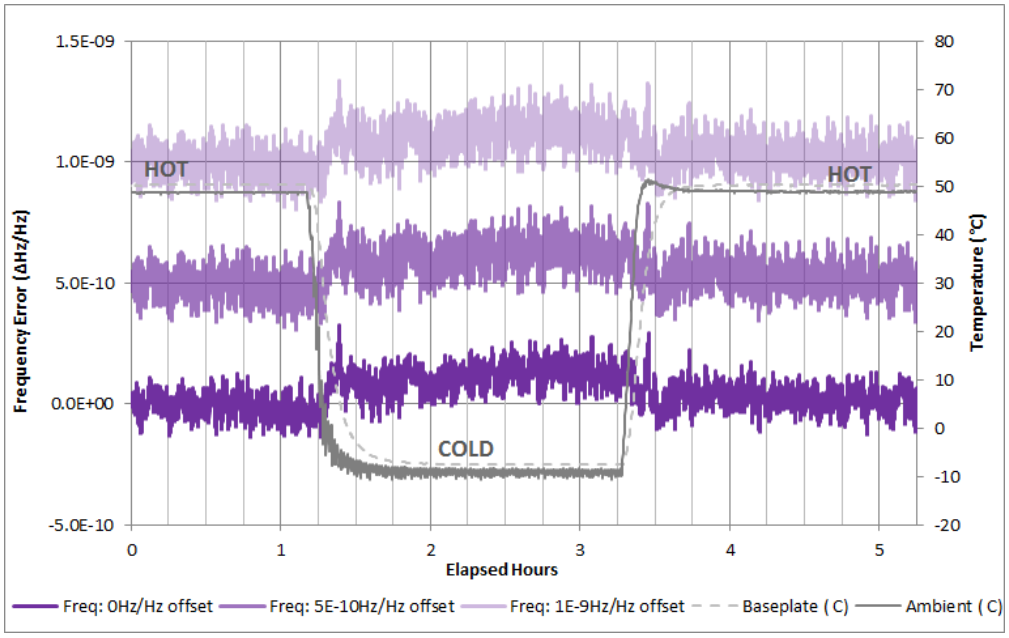
From equation 1, we can see that if a CSAC is not adequately disciplined to a superior reference prior to entering the holdover period, any frequency offset y_0 will be multiplied by the holdover duration t.

Equation 4

$$E(t) = \left(y_0 t + \frac{1}{2} a t^2\right) + \int_0^t E_i(t)dt + \varepsilon(t)$$

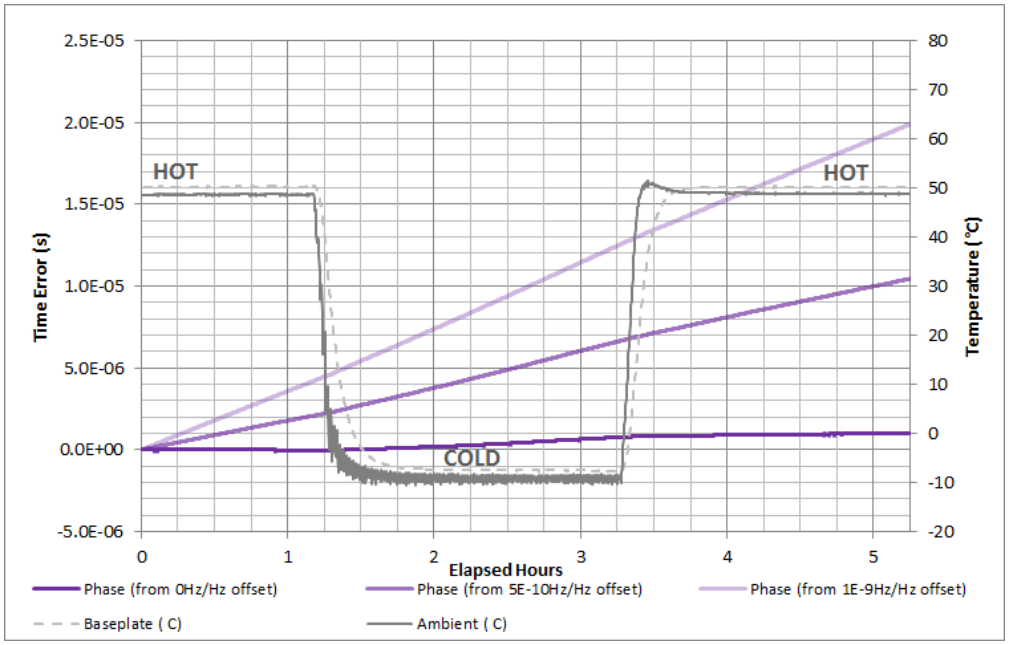
The following graph shows an example where we have taken the CSAC_1 sample data from our rapid temperature test and inserted various frequency offsets at the beginning of the data set.

Initial Frequency Error of 0, 5E–10, and 1E–9



The corresponding phase data is shown, as follows. An initial offset of 5 x 10^{-10} and 1 x 10^{-9} Hz/Hz produced 10.5 µs and 20 µs of timing error after 5 hours, respectively. This clearly masks the temperature-induced error of 1.1 µs.

Corresponding Phase Error due to Initial Frequency Error



Oscillator vs. Time Error

CSAC 1 Oscillator	2 Hours	3 Hours	5 Hours
Zero initial offset	0.1 µs	0.7 µs	1.1 µs
$5x10^{-10}$ Hz/Hz initial offset	4 µs	6 µs	10.5 µs
$1x10^{-9}$ Hz/Hz initial offset	7.5 µs	11.5 µs	20 µs

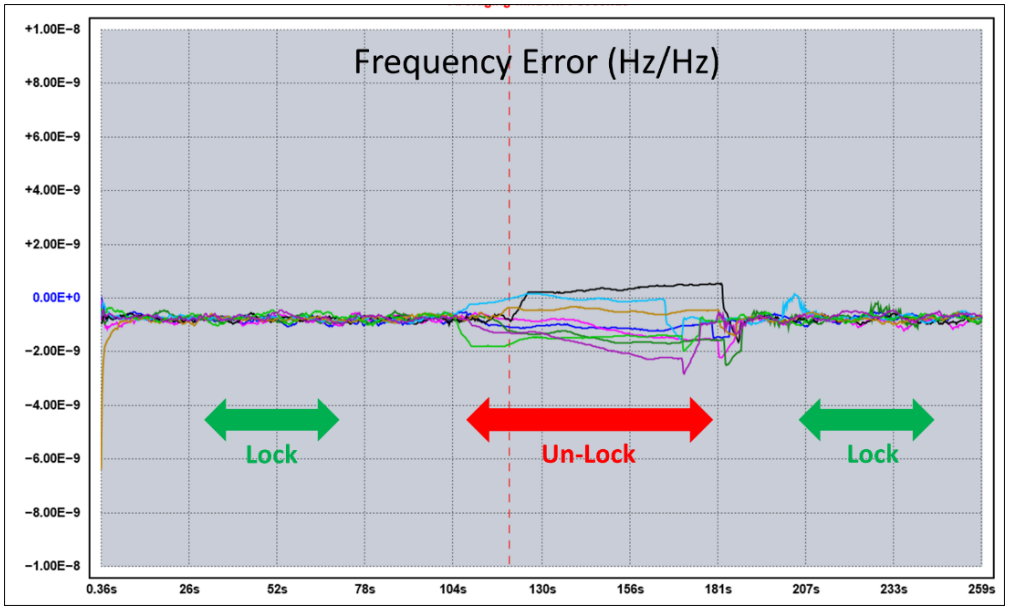
Good oscillator disciplining to minimize frequency errors is critical to achieve low holdover timing errors. Disciplining is the process of synchronizing/syntonizing an oscillator to a superior reference to remove any frequency or phase offset between the two clocks.

Effects on Timing Error: Atomic Lock Loss

A CSAC operating outside of its datasheet specifications may lose its atomic lock. If atomic lock is lost, then CSAC performance will behave per its internal TCXO. All frequency stability characteristics will be degraded accordingly: absolute frequency accuracy, drift rate, temperature stability, and vibration sensitivity will all be adversely affected. This can occur, for instance, if the vibration or temperature specification is violated. The CSAC will then attempt to re-acquire atomic lock.

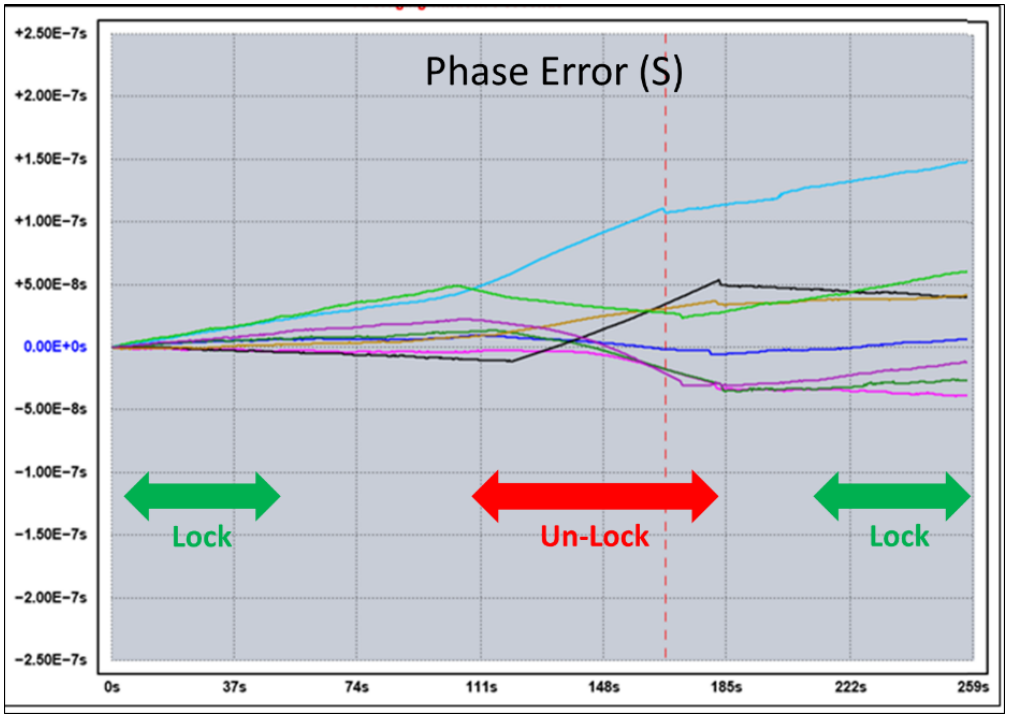
The following graph shows a CSAC that is intentionally forced to re-acquire lock (8 times). During the lock re-acquisition, the absolute frequency is offset by several parts per billion. The frequency returns to its prior offset when lock is resumed.

Frequency Offset During a Period of Lock Re-Acquisition



The following graph shows the corresponding phase error. We can see the phase error accumulate during the unlock period before returning to its locked drift rate when lock resumes. It accumulated ~60 nanoseconds of error during the ~80-second duration of unlock. It should be expected that these errors would be exacerbated if the environmental conditions were perturbed during re-acquisition.

Phase Error During a Period of Lock Re-Acquisition



Conclusion

To provide designers some guidance in typical oscillator behavior, we have demonstrated how temperature, elapsed time, initial frequency errors, and loss of atomic lock all effect the accuracy of the CSAC.

Thanks to the unique design of the CSAC, its performance in a rapidly changing temperature environment is superior to most commercial crystal oscillators and suitable for a variety of mobile applications.

References

[1] John R Vig, *Quart Crystal Resonators and Oscillators for Frequency Control and Timing Applications, a Tutorial*, FCS 1996

[2] D.B. Sullivan, *Characterisation of Clocks and Oscillators*, NIST Technical Note 1337, 1990

[3] Chang, Rassoulian, *Time Error Accumulation for SA.45s CSAC*, Microchip Doc 796-00765-000A, 2012

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