MAICMMC40X120

Datasheet

Power Core Module with SiC Power Stage

Preliminary

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Microsemi

a Microchip company

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.3

The following is a summary of the changes in revision 1.3 of this document.

- Datasheet was reorganized by major sub assembly.
- Added provisions for PCM Serial Digital Interface (PSDI) description.
- Text and value updates throughout.
- Package outlines, characteristic curves, and functional block diagram were updated

1.2 Revision 1.2

The following is a summary of the changes in revision 1.2 of this document.

- Table 13 in Pin Descriptions was updated.

1.3 Revision 1.1

The following is a summary of the changes in revision 1.1 of this document.

- The Features section was updated.
- Table 10 in Thermal Characteristics was updated.
- Table 11 in Mechanical Characteristics was updated.
- Figure 5 in Package Outlines was updated.
- Figure 6 in Package Outlines was updated.

1.4 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Product Overview

The Microsemi Power Core Module (PCM) is a 5 kVA intelligent, cost-effective module integrating the Hybrid Power Drive (HPD) module and the PCM controller. It is built on Microsemi's 35-year legacy of flight heritage and design excellence. The PCM is targeted at electric motor drives on aircraft actuator systems.

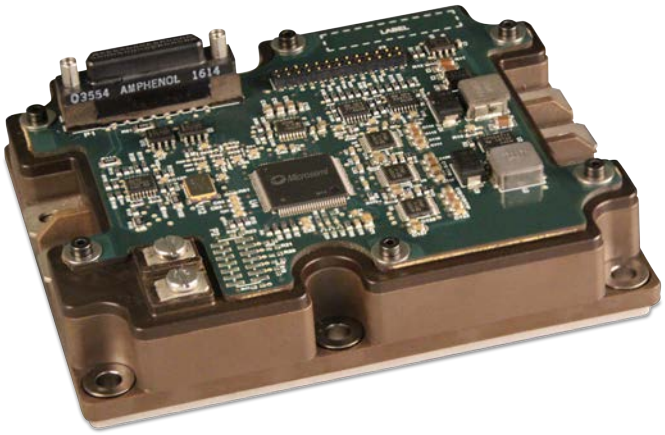
The HPD module is comprised of a power stage substrate and a driver circuit sub-assembly. The power stage of the HPD is comprised of a three-phase inverter bridge with embedded SiC MOSFETs and SiC Schottky antiparallel diodes. The driver circuit sub-assembly of the HPD is derived from Microsemi's standard HPD design. It provides a galvanically isolated interface to the power MOSFETs and their local feedback signals. It also has a solenoid driver with embedded SiC MOSFETs and SiC freewheel diode. Refer to the MAIPDMC40X120 datasheet for more information on the HPD.

The controller subassembly of the PCM is comprised of digital circuits including the Microsemi ProASIC3 FPGA. This circuitry is designed to interface with PCM Serial Digital Interface (PSDI) communication protocol and deliver the pulse width modulation (PWM) signals to the driver circuitry.

The PCM design consists of a fully integrated motor inverter driver and a solenoid driver with screw-on M3 terminals for power connections and a standard Amphenol connector interface for low-voltage signals. The module is offered in a plastic package with an AlSiC baseplate and maximum dimensions of 105.5 mm × 85.5 mm × 30 mm (right angle connector) or 105.5 mm × 85.5 mm × 36 mm (straight connector). The power substrate is potted with silicone gel and the driver printed wiring board (PWB) is Parylene coated, providing best possible environmental protection in a cost-effective, non-hermetic package.

Documentation support includes qualification and reliability data (reliability is based on FIDES guidelines).

Figure 1 • MAICMMC40X120B



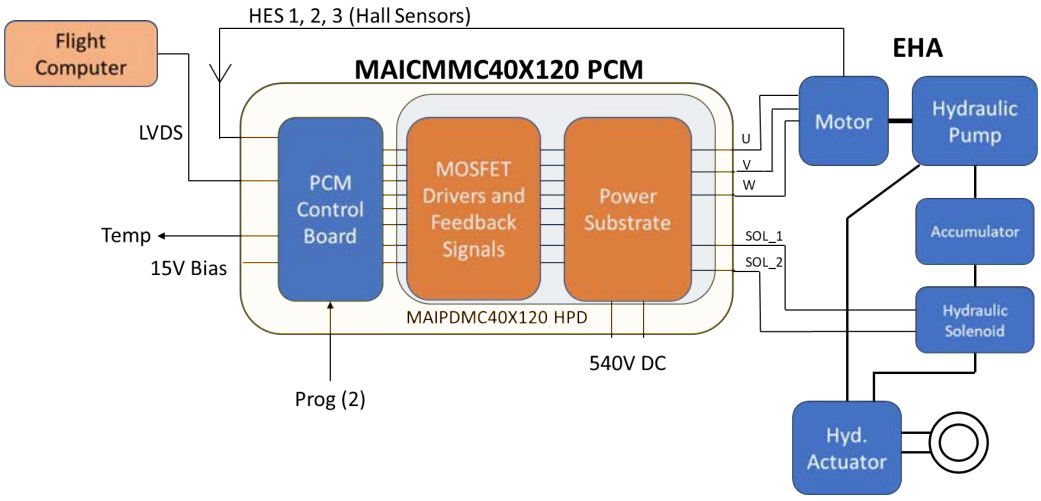
2.1 Features

The MAICMMC40X120 Power Core Module provides a fully engineered solution, offering excellent performance and reliability in electrohydrostatic actuator (EHA), electrical back-up hydraulic actuator (EBHA), and electromechanical actuator (EMA) aviation applications. The following are the key features of the MAICMMC40X120 Power Core Module:

- **Power stage**
  - SiC MOSFETs for power conversion
    - Low $R_{DS(on)}$
    - High-speed switching
    - High power efficiency
  - SiC Schottky diodes for freewheeling
    - Zero-reverse recovery
    - Temperature-independent switching behavior
- **Driver Circuit Sub-Assembly**
  - Integrated galvanically isolated gate drive circuitry
  - Circuitry for three-phase current sense, DC bus voltage sense, solenoid current sense, and temperature sense
  - SiC MOSFETs and SiC Schottky freewheel diode for solenoid driver
- **PCM Controller**
  - Integrated communication PWB with embedded ProASIC3 FPGA for digital high-speed communication and PWM output
  - High-speed low-voltage differential signaling (LVDS) communication bus for data exchange
  - Signal inputs for hall effect rotor position sensors (HES) from motor
- **Package**
  - AlSiC base plate for extended reliability and reduced weight
  - Si_3N_4 substrate for improved thermal performance and extended reliability
  - Direct mounting to heat sink (isolated package)
  - Designed for multi-sourced SiC devices, easily expandable to higher currents and technology platforms.
  - Custom variants are available; contact your Microsemi sales representative for more details.

The following illustration shows the application of a PCM within the power drive electronics system.

Figure 2 • Intelligent Power Electrical Control System (in Electro-Hydraulic Actuator (EHA))



2.2 Part Numbering

The following table shows the naming methodology for the MAICMMC40X120 Power Core Module.

Table 1 • Module Naming Methodology

M	Microsemi	
A	Screening level	A = Aviation
I	Intelligent power solutions	
CM	Type	CM = Power Core Module
MC	Technology	MC = SiC MOSFET
40	Maximum current rating in amps that MOSFETs can handle	
X	Topology	X = three-phase bridge
120	Voltage rating	120 = 1200 V
A	Package	A = right-angle connector
		B = straight connector

3 Functional Descriptions

The PCM architecture has evolved from Microsemi's standard HPD design, providing control and monitoring functionalities for motor control applications. The PCM has three parts, two of which are in the HPD—the substrate power devices and the driver circuit subassembly. The third and top part is the PCM controller subassembly. A functional block diagram of the PCM with the subassembly architecture is shown in Figure 3 below.

The PCM controller provides high-speed communication through a bidirectional LVDS interface. Two LVDS buses (i.e., the control and monitoring buses) are employed for data exchange. The control bus receiving data consists of duty cycle information for the three-phase bridge and the solenoid bridge. The control bus transmission data primarily consists of digitized PCM telemetry measurements (three-phase current, solenoid current, high-voltage direct current (HVDC) bus voltage, and rotor position signals) along with drive enable status. The monitoring bus is unidirectional (for health monitoring purposes). The transmission data for the monitoring bus is composed of PCM telemetry information with drive enable status. The PCM controller uses a Microsemi ProASIC3 FPGA to perform bidirectional LVDS communication and PWM generation.

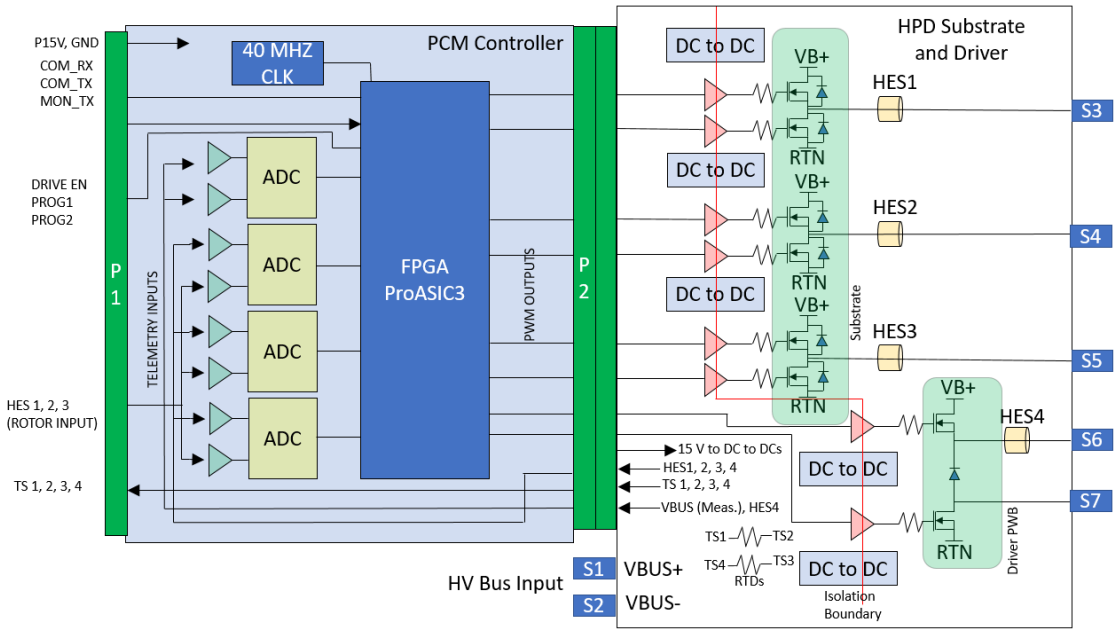
A 31-pin external connector is mounted on the PCM controller to interface the low-voltage signals with the higher level assembly. The PCM is available with two interface configurations (for more information, refer to Package Outlines).

The driver circuit subassembly within the HPD provides the gate-drive signals to the MOSFETs in the three-phase bridge and solenoid driver. There are five sets of gate-drive signals to control the SiC MOSFETs. The bias supply for the logic side of the gate drivers and other telemetry circuits is supplied by the input connector on PCM controller. The solenoid driver SiC MOSFETs and SiC Schottky antiparallel diode are located on the driver circuit subassembly along with Hall Effect Sensors (HES) to monitor the motor and solenoid currents (outputs). The driver PWB also measures the HVDC bus voltage and provides an isolated DC voltage output signal. The gate drivers, HES, and the voltage amplifier within the driver PWB provide the voltage isolation to allow reliable interface with the next level assembly. Two platinum resistive temperature transducers (PT1000) on the driver PWB monitor the HPD temperature.

The substrate contains 1200 V–rated, high-speed SiC MOSFETs and SiC Schottky antiparallel diodes to generate the three-phase switching outputs. Power and low-level signal routing is provided through pin terminals from the driver PWB to the substrate.

The following illustration shows the functional blocks of the MAICMMC40X120 Power Core Module.

Figure 3 • Functional Block Diagram



4 Electrical Specifications

This section shows the electrical specifications for the MAICMMC40X120 Power Core Module device.

4.1 Absolute Maximum Ratings

This section shows the absolute maximum ratings of the MAICMMC40X120 Power Core Module device.

Table 2 • Absolute Maximum Ratings

Symbol	Parameter		Ratings	Unit
V_{DSS}	Drain-source breakdown voltage		1200	V
I_D	Continuous switch drain current	T_C = 25 °C	63	A
		T_C = 100 °C	46	A
I_{DM}	Pulsed drain current		160	A
I_F	Antiparallel diode maximum DC forward current	T_J = 25 °C	43	A
P15V	Input bias1 supply voltage		18	V
I_{CC}	Input bias1 supply current (at 12 V)		250	mA
V_{DISC}	Discrete signal input voltage		3.6	V
V_{LVDS}	LVDS bus voltage range		–0.5 to 3.3	V
T_J	Maximum power semiconductor junction temperature		175	°C

4.2 Typical Electrical Performance

The following table shows the input electrical characteristics of the MAICMMC40X120 Power Core Module at 25 °C unless otherwise specified.

Table 3 • Input Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Steady-state HVDC input voltage	VBUS		540	750	V	
Bias1 power supply voltage	P15V	12	15	18	V	
Bias1 supply current	ICC		140		mA	F_{SW}[1] = 10 kHz
Rotor position measurement range	HES_IN	0		24	mA	Hall Effect Sensor
Discrete signal input voltage	VDISC	0	3.3	3.6	V	PROG1; PROG2; DRIVE_EN[2]

Note:

1. F_{SW} corresponds to the switching frequency.
2. GND/open low-power circuit; ground state: voltage < 0.9 V at 1 mA; open state: equivalent impedance > 1 MΩ

The following table shows the output electrical characteristics of the MAICMMC40X120 Power Core Module at 25 °C unless otherwise specified.

Table 4 • Output Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Phase current	Peak amplitude	I_{ph}			12.5	A	F_{SW} = 10 kHz T_C = 110 °C HVDC = 540 VDC
					25		F_{SW} = 10 kHz T_C = 95 °C HVDC = 540 VDC
Solenoid current	Steady state	SOL_SW-SS		1		A	F_{SW} = 10 kHz T_C = 110 °C HVDC = 540 VDC
	Transient	SOL_SW-T		5			F_{SW} = 10 kHz T_C = 110 °C HVDC = 540 VDC For <100 ms
Power rating		P_{OUT}		5		kVA	
Switching voltage transient rate		dV_{DS}/dt		16		kV /µs	F_{SW} = 10 kHz HVDC = 540 VDC I_D = 12.5 A
Power efficiency		η		99.5		%	F_{SW} = 10 kHz T_C = 20 °C HVDC = 540 VDC I_D = 12.5 A MI = 0.98 CosΦ = 0.87
Phase current sense range		I_{PR}	–40		40	A	
Solenoid current sense range		I_{SR}	–10		10	A	
Full-scale current sense accuracy		I_{TOT}		Motor current	12.8	%	T_A = –55 °C to 110 °C
				Solenoid	10.6		T_A = –55 °C to 110 °C
Full-scale HVDC sense accuracy accuracy					3.0	%	T_A = –55 °C to 110 °C
Rotor position accuracy					2.0	%	T_A = –55 °C to 110 °C
Rotor position current-conversion factor		RP_F		1 LSB = 10 µA			2’s complement encoding
Phase current-digital conversion factor		IP_F		–200 A to 200 A = 8000h to 7FFFh			2’s complement encoding
Solenoid current-digital conversion factor		IS_F		–200 A to 200 A = 8000h to 7FFFh			2’s complement encoding
HVDC input bus-conversion factor		DC_F		–1000V to 1000 V = 8000h to 7FFFh			2’s complement encoding

The following table shows the LVDS signal characteristics of the MAICMMC40X120 Power Core Module at 25 °C unless otherwise specified.

Table 5 • LVDS Signal Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
LVDS high-level input voltage	VLVDS_H	2			V
LVDS low-level input voltage	VLVDS_L			0.8	V
Differential input voltage	VLVDS_ID	0.1		0.6	V
Common-mode output voltage	VLVDS_OCM	1.125	1.2	1.375	V
Differential output voltage	VLVDS_OD	247	340	454	mV

The following table shows the SiC MOSFET characteristics of the MAICMMC40X120 Power Core Module at 25 °C unless otherwise specified. The SiC MOSFET characteristics listed in Table 6 are bare die measurements. This data is for analysis only and has not been validated in the PCM package.

Table 6 • SiC MOSFET Die Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Drain-source on resistance	$R_{DS(on)}$		40	52	mΩ	V_{GS} = 20 V T_C = 25 °C I_D = 40 A
Turn-on delay time	$T_{d(on)}$		15		ns	V_{GS} = 20/–5 V V_{Bus} = 800 V I_D = 40 A R_G = 2.5 Ω Inductive switching
Turn-off delay time	$T_{d(off)}$		26			
Rise time	T_r		52			
Fall time	T_f		34			
Turn-on energy	E_{on}		1		mJ	
Turn-off energy	E_{off}		0.4			

The following table shows the body diode and SiC freewheeling diode characteristics of the MAICMMC40X120 Power Core Module at 25 °C unless otherwise specified. The SiC diode characteristics listed in Table 7 are bare die measurements. This data is for analysis only and has not been validated in the PCM package.

Table 7 • Body Diode and SiC Freewheeling Diode Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Body diode forward voltage	VSD		4.1		V	V_{GS} = –5 V I_{SD} = 20 A T_J = 25 °C
Body diode reverse recovery time	t_{rr}		54		ns	ISD = 40 A VGS = –5 V VR = 800 V diF/dt = 1000 A/µs T_J = 25 °C
Body diode reverse recovery charge	Q_{rr}		283		nC	
Body diode reverse recovery current	I_{rr}		15		A	
Peak repetitive reverse voltage	V_{RRM}			1200	V	
Freewheeling diode forward voltage	V_F		1.5	1.8	V	I_F = 10 A T_J = 25 C
			2.3		V	I_F = 10 A T_J = 175 C

The following table shows the isolation characteristics of the MAICMMC40X120 Power Core Module at 25 °C unless otherwise specified.

Table 8 • Isolation Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Gate driver common-mode transient immunity (CMTI)	$\lvert dV_{ISO}/dt \rvert$			100	kV/µs	V_{CM} = 1 kV
RMS isolation voltage, any terminal to case t = 1 min, 50 Hz/60 Hz	V_{ISOL1}	1500			V_{RMS}	
Isolation dielectric between power and control stage under DC voltage	V_{ISOL2}	2120			V_{DC}	
Isolation resistance between power and control stage under 500 VDC	V_{ISOL3}	100			MΩ	

The following table shows the temperature sensor PTC characteristics of the MAICMMC40X120 Power Core Module at 25 °C unless otherwise specified. Use the values in the following table to calculate the thermistor value (R_T):

$R_T = R_0(1 + A \cdot T + B \cdot T^2)$ for the temperature range from 0 °C to 250 °C

$R_T = R_0(1 + A \cdot T + B \cdot T^2 + C(T - 100)T^3)$ for the temperature range from –55 °C to 250 °C

Table 9 • Temperature Sensor PTC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Temperature sense range	T_R	–55		250	°C	
RTD nominal value	R_0		1000		Ω	At 0 °C
Temperature sense accuracy	T_{TOT}	–2		2	°C	
	A		3.9083×10^{-3}		$°C^{-1}$	
	B		-5.775×10^{-7}		$°C^{-2}$	
	C		-4.183×10^{-12}		$°C^{-4}$	
	ΔT					As per IEC60751 Class A

5 Thermal Characteristics

The following table shows the thermal characteristics of the MAICMMC40X120 Power Core Module.

Table 10 • Thermal Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Case temperature	T_C	–55		110	°C	Refer to derating curves in Characteristic Curves
Storage	T_S	–55		125	°C	
Pressure range		11.6		190	kPa	
Thermal resistance (junction-case)	$\Theta_{JC\ MOSFET}$			0.77	°C/W	
	$\Theta_{JC\ DIODE}$			0.67		
Power dissipation			25		W	F_{SW} = 10 kHz T_C = 20 °C CosΦ = 0.97 V_{BUS} = 540 V I_D = 12.5 A

6 Mechanical Characteristics

The following table shows the mechanical characteristics of the MAICMMC40X120 Power Core Module. Use caution as these devices are sensitive to electrostatic discharge. Be sure to follow proper handling procedures.

Table 11 • Mechanical Characteristics

Parameter	Max	Unit
Size: MAICMMC40X120A	105.5 × 85.5 × 30	mm
Size: MAICMMC40X120B	105.5 × 85.5 × 36	mm
Mass	300	g
Mounting: fastener	4.4 Ø (×6) (through-hole)	mm
Mounting: washer	9.0 Ø (×6) (surface)	mm
Mounting torque: M4 (to heat sink)	1.2–3.5	Nm
Power connector	M3 screw terminals (×7)	
Mounting torque: power connector	0.9–1	Nm
Signal connector part number: MAICMMC40X120A	102R31P-CBRPT1	
Signal connector part number: MAICMMC40X120B	102R31P-C6P1	
Baseplate information	AlSiC material with thickness: 4 mm	

7 Characteristic Curves

The following illustrations show the characteristic curves of the MAICMMC40X120 Power Core Module.

Figure 4 • Thermal Derating Curve

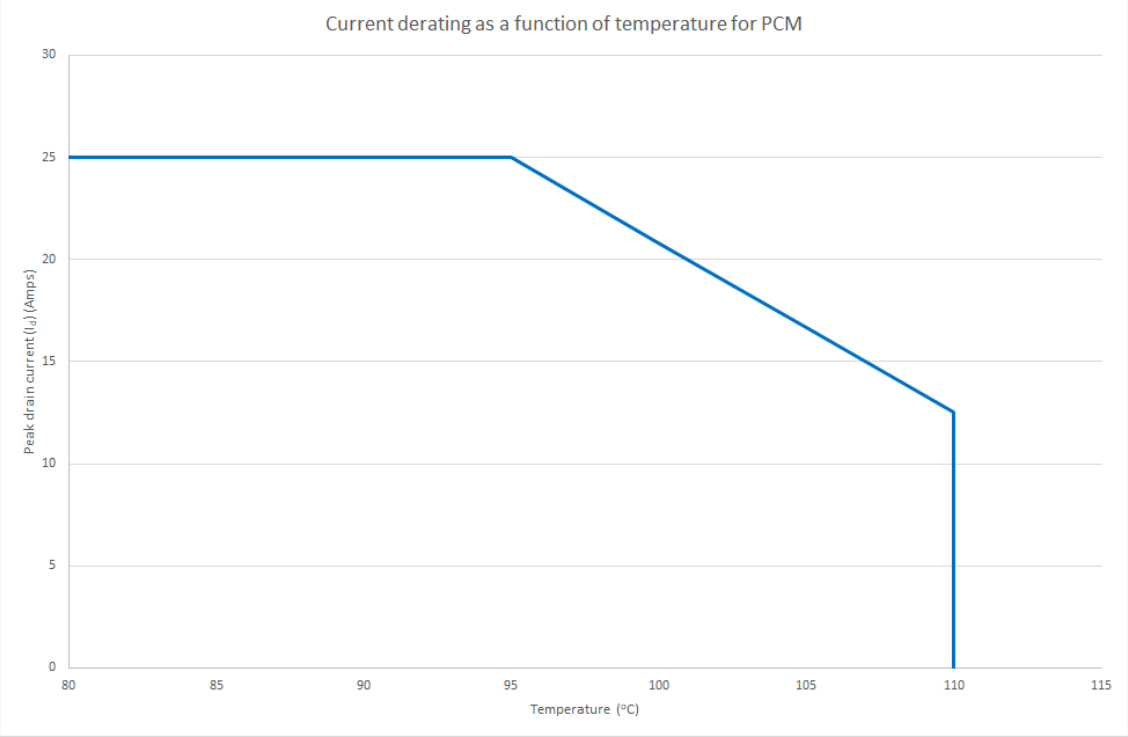


Figure 5 • Altitude Derating Curve

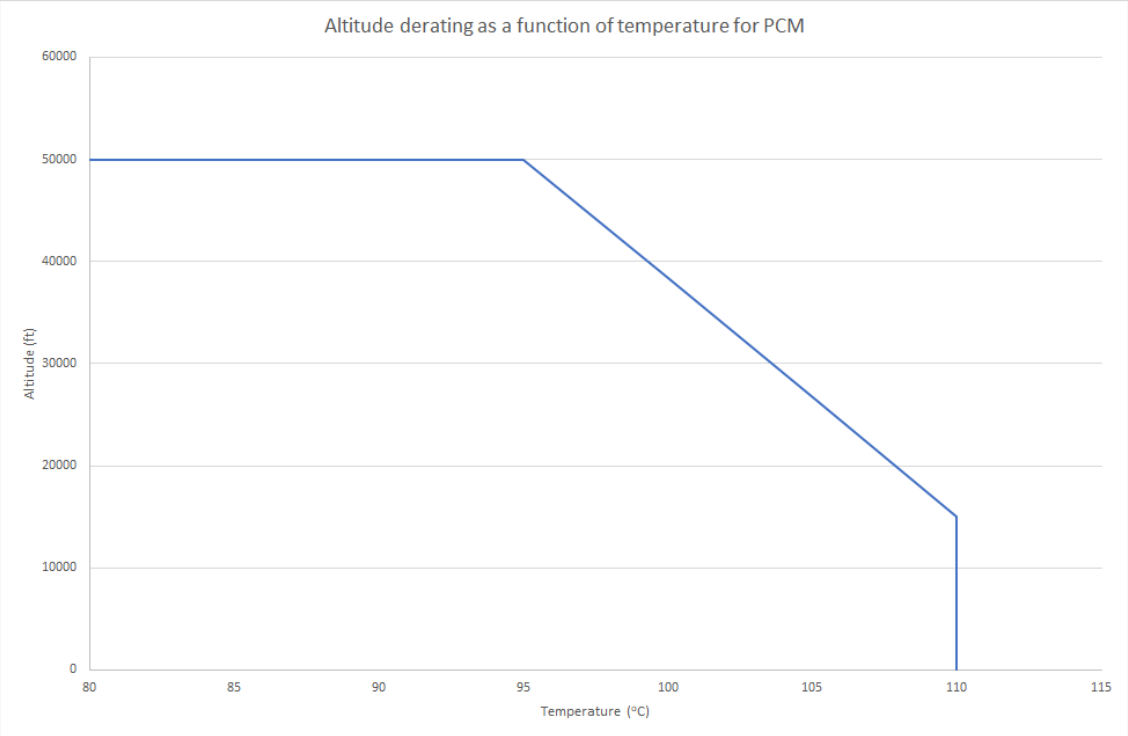
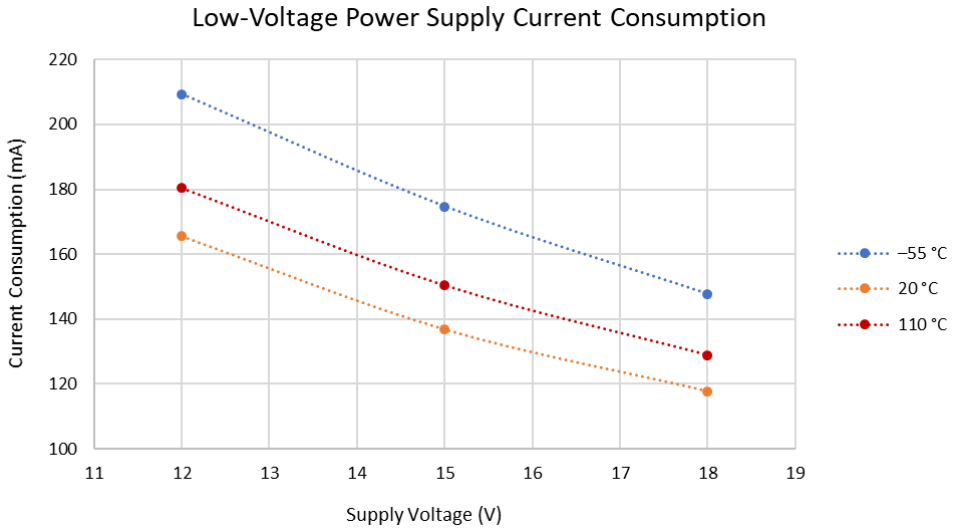


Figure 6 • Bias Current vs. Supply Voltage Over Temperature Curve



8 Pin Descriptions

The following table shows the power pin descriptions for the MAICMMC40X120 Power Core Module.

Table 12 • Power Pin Descriptions

Power pin	Description	Reference	I/O Type	Connector Type
S1	HVDC bus input	V_BUS +	Input	M3 screw terminal
S2	HVDC bus input return	V_BUS –	Input	M3 screw terminal
S3	Output current for phase	Phase_U	Output	M3 screw terminal
S4	Output current for phase	Phase_V	Output	M3 screw terminal
S5	Output current for phase	Phase_W	Output	M3 screw terminal
S6	Solenoid output current	Sol_1	Output	M3 screw terminal
S7	Solenoid output current return	Sol_2	Output	M3 screw terminal

The following table shows the signal pin descriptions for the MAICMMC40X120A and MAICMMC40X120B Power Core Module. MAICMMC40X120A and MAICMMC40X120B configurations have the same signal pin-out as listed below.

Table 13 • MAICMMC40X120 Signal Pin Descriptions

P1 Signal Pin	Description	Designator	I/O Type	Signal Definition
1	HES rotor input2	HES_IN2	Input	Analog input range: 0 mA–24 mA
2	Ground	GND	Input	
3	HES rotor input3 return	HES_IN3_RTN	Input	Return for HES rotor input3
4	Ground	GND	Input	
5	Do not connect	Not applicable	Reserved	Reserved
6	Ground	GND	Input	
7	Do not connect	Not applicable	Reserved	Reserved
8	Ground	GND	Input	
9	Temperature sensor (1) +	TEMP_SENSOR1+	Output	Refer to Temperature Sensor table
10	Control bus (LVDS_N) receive signal return	COM_RX_N	Input	Refer to LVDS Signal Characteristics table
11	Temperature sensor (1) –	TEMP_SENSOR1–	Output	Refer to Temperature Sensor table
12	Reserved for FPGA programming through JTAG	Not applicable	Reserved	Reserved
13	Temperature sensor (2) +	TEMP_SENSOR2+	Output	Refer to Temperature Sensor table
14	Reserved for FPGA programming through JTAG	Not applicable	Reserved	Reserved
15	Temperature sensor (2) –	TEMP_SENSOR2–	Output	Refer to Temperature Sensor table
16	15 V bias input	P15V	Input	15 VDC power source
17	HES rotor input2 return	HES_IN2_RTN	Input	Return for HES rotor input2
18	Do not connect	Not applicable	Reserved	Reserved
19	HES rotor input3	HES_IN3	Input	Analog input range: 0 mA–24 mA
20	Do not connect	Not applicable	Reserved	Reserved

P1 Signal Pin	Description	Designator	I/O Type	Signal Definition
21	HES rotor input1	HES_IN1	Input	Analog input range: 0 mA–24 mA
22	HES rotor input1 return	HES_IN1_RTN	Input	Return for HES rotor input1
23	Status bus (LVDS_N) transmit signal return	MON_TX_N	Output	Refer to LVDS Signal Characteristics table
24	Do not connect	Not applicable	Reserved	Reserved
25	Status bus (LVDS_P) transmit signal	MON_TX_P	Output	Refer to LVDS Signal Characteristics table
26	Control bus (LVDS_P) receive signal	COM_RX_P	Input	Refer to LVDS Signal Characteristics table
27	Pin programming 2	PROG2	Input	GND/open low-power circuit Ground state: voltage < 0.9 V at 1 mA Open state: equivalent impedance > 1 MΩ
28	Control bus (LVDS_N) transmit signal return	COM_TX_N	Output	Refer to LVDS Signal Characteristics table
29	Pin programming 1	PROG1	Input	GND/open low-power circuit Ground state: voltage < 0.9 V at 1 mA Open state: equivalent impedance > 1 MΩ
30	Drive enable	DRIVE_EN	Input	GND/open low-power circuit Ground state: voltage < 0.9 V at 1 mA Open state: equivalent impedance > 1 MΩ
31	Control bus (LVDS_P) transmit signal	COM_TX_P	Output	Refer to LVDS Signal Characteristics table

Note: The mating connector is TE Connectivity part number TBD.

The following image shows the P1 signal pin locations for the MAICMMC40X120 Power Core Module.

Figure 7 • P1 Signal Pin Locations

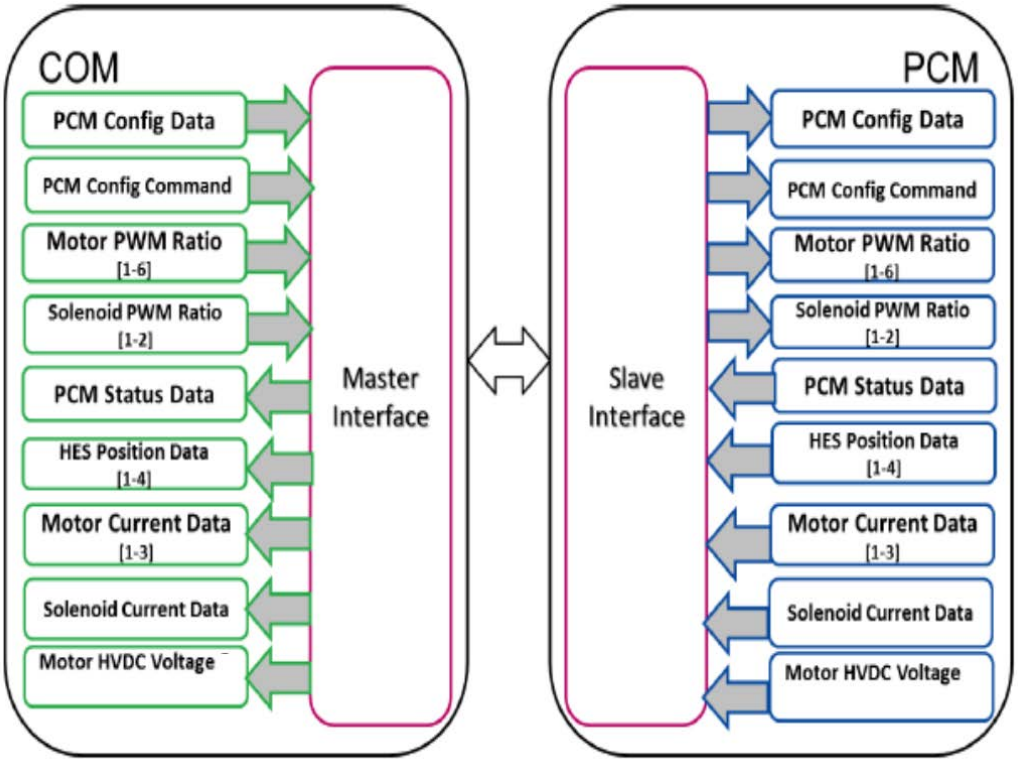
9 Serial Communication Description

This section describes the serial communication function of the MAICMMC40X120 Power Core Module.

9.1 Functional Description

The external serial digital command module (COM) transmits commands to the PCM to generate the PWM controls for the three-phase bridge and solenoid drive. The PSDI is designed to replace conventional analog and digital interfaces with a serial digital channel. The functional block diagram of the PSDI is shown in the following figure.

Figure 8 • Communications Interface



9.2 PSDI Bus Characteristics

The following are characteristics of the PSDI Bus:

- The physical layer is based on point-to-point transmit and receive links at LVDS levels.
- Manchester encoding is used.
- LVDS receivers provide an impedance of 100 Ω.
- Data bit rate is at 20 MHz. Data exchange is periodic with a cycle time of 100 µs.
- A "0" data bit is represented by a low for 25 ns follow by a high for 25 ns.
- A "1" data bit is represented by a high-to-low transition of inverse timing.
- Each message is composed of three header words and eleven payload words followed by one CRC word
- The last word in the payload message is the CRC word for error detection of the transmitted message
- The CRC polynomial being used for the CRC calculation is 1021h

9.3 PSDI Functional Definitions

The following are the PSDI functional definitions of the PCM device:

- The COM is defined as the master module, while the PCM is defined as the slave module.
- All data exchanges are initiated by the master through master messages.
- The slaves transmit slave messages only when commanded by the master.

9.4 PSDI Operating Modes

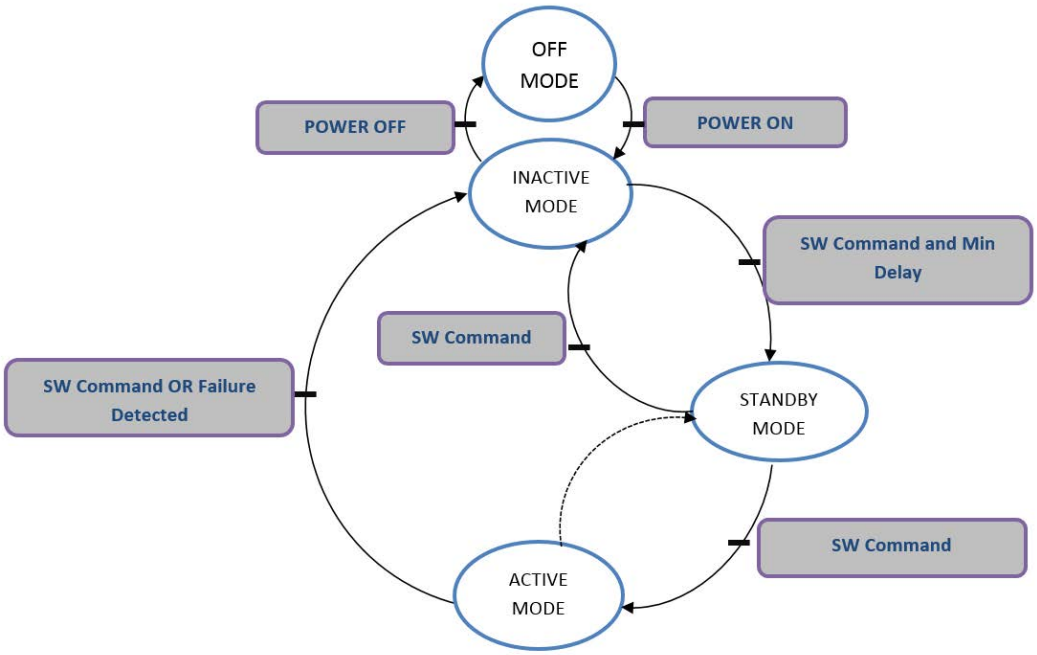
The four PSDI operating modes consist of the following: OFF Mode, INACTIVE Mode, STANDBY Mode, and ACTIVE Mode. The design transition state flow diagram is shown in the PSDI State Flow Chart.

The following list describes PSDI operating modes:

- OFF Mode: In OFF mode, there is no communication between the PCM and COM.
- INACTIVE Mode: In INACTIVE mode, power is applied but there is no communication between the PCM and the COM. After power-up, the PCM is in an inactive state waiting for the master-initialization message.
- STANDBY Mode: The COM generated the initialization message to the PCM. Upon receiving the initialization message, the PCM transitions into the STANDBY mode and transmits back the slave descriptor message. The COM validates the slave descriptor message and transmits the PWM command message to the PCM.
- ACTIVE Mode: Upon receiving the PWM command message from the COM, the PCM enters the ACTIVE state and sends back the data acquisition message. This process is repeated every time a new PWM command message is received.
- If consecutive transmission errors are detected, the PCM returns to the INACTIVE mode. A master command is needed to bring the PCM out of INACTIVE mode.

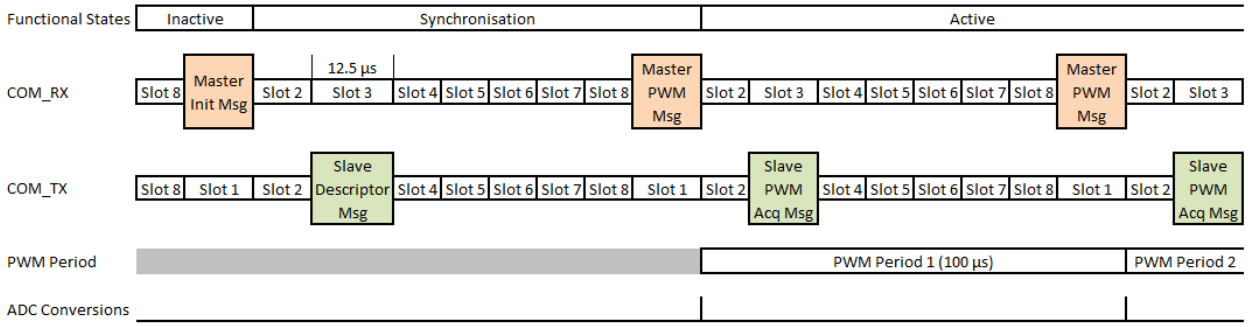
The following image shows the PSDI state flow chart of the MAICMMC40X120 Power Core Module.

Figure 9 • PSDI State Flow Chart



The following image shows the PSDI operating timeline of the MAICMMC40X120 Power Core Module.

Figure 10 • PSDI Operating Timeline



Message Type Code	Source	Message
0000	Master	Sync
0001	Master	PWM
1000	Slave	Descriptor
1001	Slave	PCM Acquisitions

9.5 PSDI Message Definitions

There are two types of master command messages and two types of slave return message being transmitted on the PSDI in the following sequence:

1. The Master Sync message commands the PDC operating mode and the initialization message.
2. The PCM will return the Slave Description message back to the master once the Master Init message is received.
3. The other command message being sent to the PCM is the Master PWM message. This message informs the PCM of the PWM ratios that should be applied to the switches to generate the three-phase and solenoid drive currents. Note that the PCM shall generate the complementary PWM ratios for all bottom switches and insert dead time on the output transitions.
4. Upon receiving the Master PWM message, the PCM starts the next PWM cycle, performs ADC conversions to gather telemetry data, and sends out the Slave Acquisition message that contains telemetry and status information.

The following figures show detailed descriptions of the four PSDI message types.

Figure 11 • Master Sync Message

#	Word Description	MSB b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	LSB b0
1	Start of frame	1	1	1	1	0	0	0	0	1	1	0	0	1	1	0	0
2	Header word 2	1	1	1	0	0	0	0	0	0	0	0	0	1	0	X	X
			Source ID			↑ Slave frame type		Frame Subtype		Start of cycle indication				Frame destination			
3	Header word 3	1	0	0	0	Y	Y	Y	Y	Y	Y	Y	Y	0	0	0	0
			Slave message request					PICOL cycle count							Slot number		
4	Payload word 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
								Initialization message									
5	Payload word 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	Payload word 3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	Payload word 4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	Payload word 5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	Payload word 6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	Payload word 7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	Payload word 8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	Payload word 9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	Payload word 10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	Payload word 11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	CRC of words 1 - 14	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Figure 12 • Master PWM Message

#	Word Description	MSB b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	LSB b0
1	Start of frame	1	1	1	1	0	0	0	0	1	1	0	0	1	1	0	0
2	Header word 2	1	1	1	0	0	0	0	1	0	0	0	0	1	0	X	X
		Source ID				↑ Slave frame type	Frame Subtype			Start of cycle indication				Frame destination			
3	Header word 3	1	0	0	0	Y	Y	Y	Y	Y	Y	Y	Y	0	0	0	0
		Slave message request				PICOL cycle count								Slot number			
4	PWM1 high side	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		↑ Safe state ("0" => Inverter/Solenoid open, "1" => Normal operation)	↑ Dead time ("0" => No dead time, "1" => Inserted dead time)	↑ PWM shape ("0" => Asymmetric, "1" => Symmetric)	↑ PWM signal polarity ("0' => Inverted, "1" => Normal)	PWM ratio ("000h" => 0%, "FFFh" => 100%)											
5	PWM1 low side	To be Ignored															
6	PWM2 high side	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
7	PWM2 low side	To be Ignored															
8	PWM3 high side	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
9	PWM3 low side	To be Ignored															
10	Solenoid high side	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
11	Solenoid low side	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
12	Bridge dynamic config	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X
		Provision												Max # of consecutive error			
13	Payload word 10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	Payload word 11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	CRC of words 1 - 14	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Figure 13 • Slave Descriptor Message

#	Word Description	MSB b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	LSB b0
1	Start of frame	1	1	1	1	0	0	0	0	1	1	0	0	1	1	0	0
2	Header word 2	0	0	0	1	1	0	0	0	X	X	X	X	X	X	X	X
		Source ID				↑ Slave frame type	Frame Subtype			PCM status							
3	Header word 3	X	X	X	X	Y	Y	Y	Y	Y	Y	Y	Y	0	0	0	0
		PCM status				PICOL cycle count								Slot number			
4	Payload word 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		Provision												PCM module size			
5	Payload word 2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
		OTAN code															
6	Payload word 3	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
		PCM part number															
7	Payload word 4	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
		PCM serial number															
8	Payload word 5	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
		PWM2 dead time (1 LSB => 10 ns)								PWM1 dead time (1 LSB =>10 ns)							
9	Payload word 6	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
		Solenoid dead time (1 LSB => 10 ns)								PWM3 dead time (1 LSB => 10 ns)							
10	Payload word 7	0	0	0	1	1	0	0	1	0	0	0	0	1	0	1	0
		PCM max output current (12 A to 100 A, LSB = 1 A)								PCM max output power (5 kW to 41 kW, LSB = 500 W)							
11	Payload word 8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	Payload word 9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	Payload word 10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	Payload word 11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	CRC of words 1 - 14	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Figure 14 • Slave PCM Acquisition Message

#	Word Description	MSB b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	LSB b0
1	Start of frame	1	1	1	1	0	0	0	0	1	1	0	0	1	1	0	0
2	Header word 2	0	0	0	1	1	0	0	1	X	X	X	X	X	X	X	X
		Source ID				↑ Slave frame type	Frame Subtype			PCM status							
3	Header word 3	X	X	X	X	Y	Y	Y	Y	Y	Y	Y	Y	0	0	0	0
		PCM status				PICOL cycle count								Slot number			
4	Payload word 1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
		N/A															
5	Payload word 2	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		PCM HVDC Voltage (–1000 V to 1000 V, "8000h" to "7FFFh")															
6	Payload word 3	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		PCM Phase 1 Current (–200 A to 200 A, "8000h" to "7FFFh")															
7	Payload word 4	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		PCM Phase 2 Current (–200 A to 200 A, "8000h" to "7FFFh")															
8	Payload word 5	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		PCM Phase 3 Current (–200 A to 200 A, "8000h" to "7FFFh")															
9	Payload word 6	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		Solenoid Current (–200 A to 200 A, "8000h" to "7FFFh")															
10	Payload word 7	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		Rotor Position 1 (LSB = 1 mV)															
11	Payload word 8	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		Rotor Position 2 (LSB = 1 mV)															
12	Payload word 9	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		Rotor Position 3 (LSB = 1 mV)															
13	Payload word 10	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		PCM status (TBD)															
14	Payload word 11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Provision															
15	CRC of words 1 - 14	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

10 Package Outlines

The following illustrations show the package outlines for the MAICMMC40X120A and MAICMM4C0X120B Power Core Module variants.

Figure 15 • Package A Outline

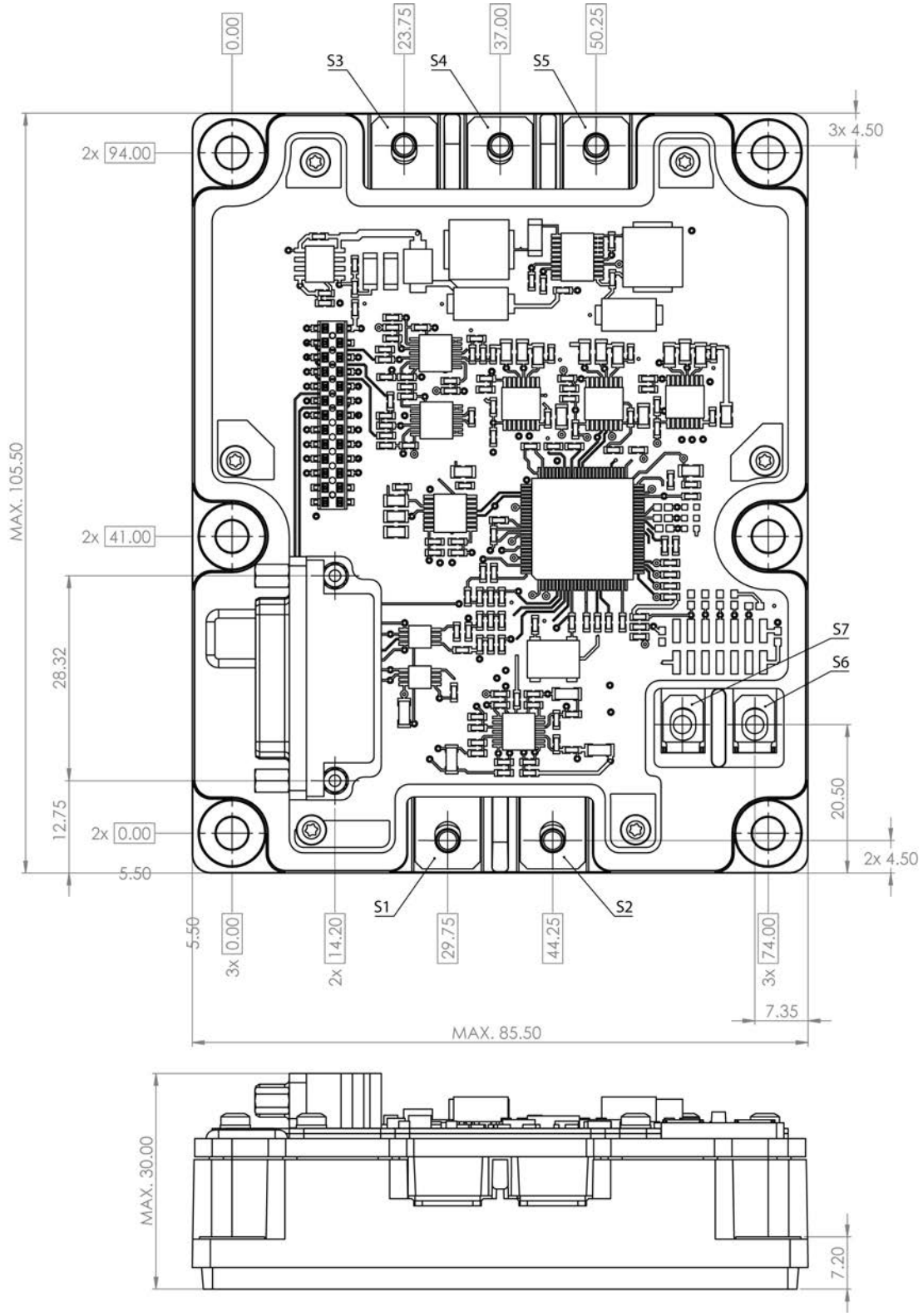
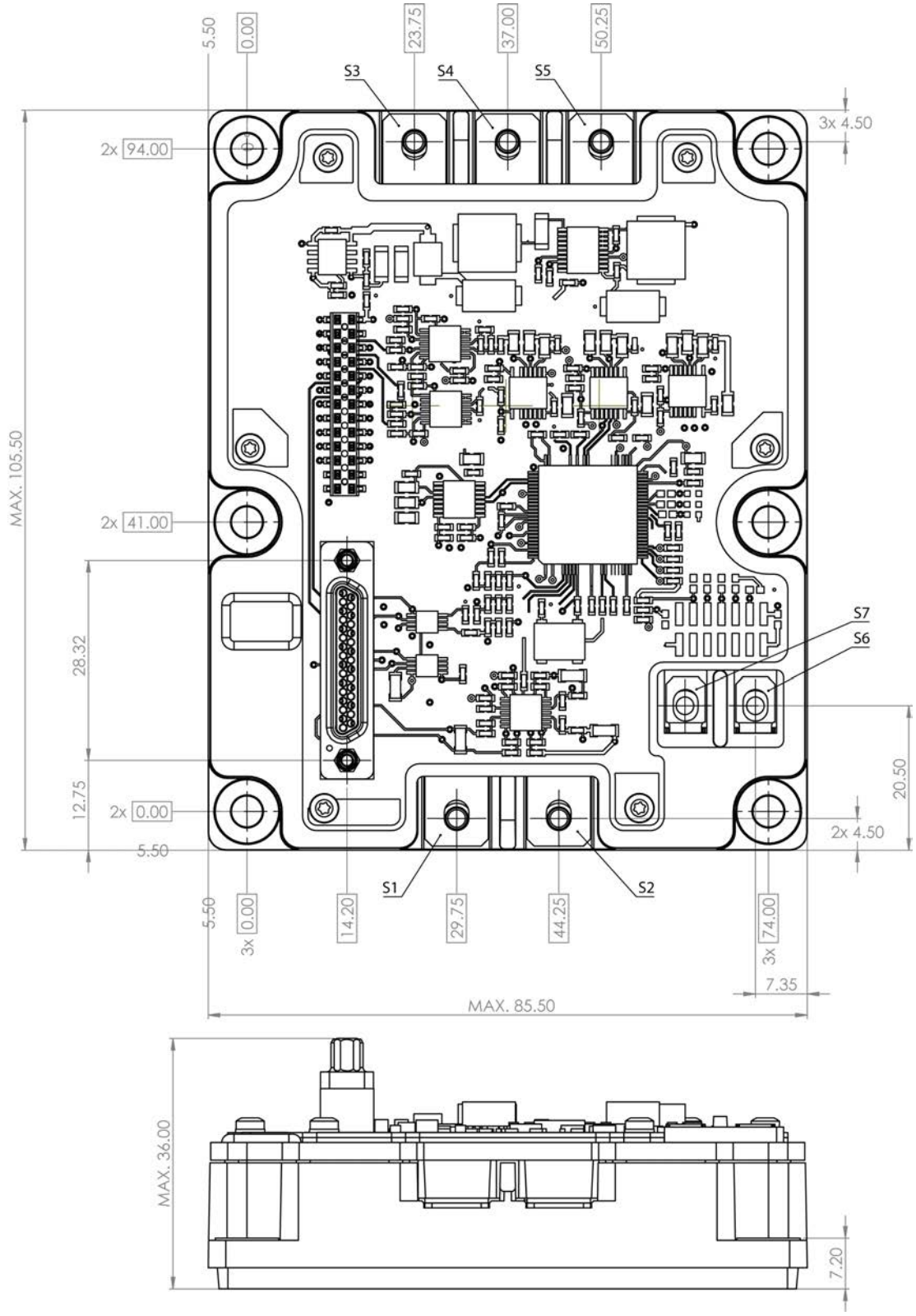


Figure 16 • Package B Outline



Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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