RELIABILITY REPORT

FOR

MAX3671ETN+ (MAX3673)

PLASTIC ENCAPSULATED DEVICES

June 8, 2009

## MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Approved by	
Ken Wendel	
Quality Assurance	
Director, Reliability Engineering	

### Conclusion

The MAX3671ETN+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

#### **Table of Contents**

I	Devi	ce D	escri	ption	VQuality Assurance Information

- II. ......Manufacturing Information
- VI. ......Reliability Evaluation
- III. ......Packaging Information
- .....Attachments

IV. .....Die Information

#### I. Device Description

A. General

The MAX3671/ MAX3763 are low-jitter frequency synthesizers that accepts two reference clock inputs and generates nine phase-aligned outputs. The device features 40kHz jitter transfer bandwidth, 0.3psRMS (12kHz to 20MHz) integrated phase jitter, and best-in-class power-supply noise rejection (PSNR), making it ideal for jitter cleanup, frequency translation, and clock distribution in Gigabit Ethernet applications. The MAX3671 / MAX3673 operate from a single +3.3V supply and typically consumes 400mW. The IC is available in an 8mm x 8mm, 56-pin TQFN package, and operates from -40°C to +85°C.

## II. Manufacturing Information

- A. Description/Function:Low-Jitter Frequency Synthesizer with Selectable Input ReferenceB. Process:MB3C. Number of Device Transistors:CaliforniaD. Fabrication Location:California
- E. Assembly Location:UTL ThailandF. Date of Initial Production:January 31, 2009

## III. Packaging Information

A. Package Type:	56-pin TQFN 8x8
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Au (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	35°C/W
K. Single Layer Theta Jc:	0.6°C/W
L. Multi Layer Theta Ja:	21°C/W
M. Multi Layer Theta Jc:	0.6°C/W

#### IV. Die Information

A. Dimensions:	111 X 111 mils
B. Passivation:	BCB
C. Interconnect:	2 x Aluminum/Cu (Cu = 0.5%), top layer 100% Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35 um
F. Minimum Metal Spacing:	0.35 um
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Saw

#### V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

#### VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are pending. Using these results, the Failure Rate  $(\lambda)$  is calculated as follows:

 $\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{169007 \times 1555 \times 2} \text{ (Chi square value for MTTF upper limit)}$  (where 1555 = Temperature Acceleration factor assuming an activation energy of 0.7eVand 169007 = Device Hrs at Stress, 135°C)  $\lambda = 2.3 \times 10^{-9}$ 

x = 2.3 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the MB3HT Process results in a FIT Rate of 0.7 @ 25C and 11.5 @ 55C (0.7 eV, 60% UCL)

#### B. Moisture Resistance Tests

The industry standard  $85^{\circ}C/85\%$ RH or HAST testing is monitored per device process once a quarter.

#### C. E.S.D. and Latch-Up Testing

The HT59 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA, 1.5x VCCMax Overvoltage per JESD78.

# Table 1 Reliability Evaluation Test Results

## MAX3671ETN+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	
Static Life Test	(Note 1)				
	Ta = 135°C	DC Parameters	466	0	
	Biased	& functionality			
	Time = mixed hrs				
Moisture Testing	(Note 2)				
85/85	Ta = 85°C	DC Parameters	77	0	
	RH = 85%	& functionality			
	Biased				
	Time = 1000hrs.				
Mechanical Stres	ss (Note 2)				
Temperature	-65°C/150°C	DC Parameters	77	0	
Cycle	1000 Cycles	& functionality			
	Method 1010				

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data