RELIABILITY REPORT

FOR

MAX3674ECM+

PLASTIC ENCAPSULATED DEVICES

June 29, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX3674ECM+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX3674 is a high-performance network clock synthesizer IC for networking, computing, and telecom applications. It integrates a crystal oscillator, a low-noise phase-locked loop (PLL), programmable dividers, and high-frequency LVPECL output buffers. The PLL generates a high-frequency clock based on a low-frequency reference clock provided by the on-chip crystal oscillator or an external LVCMOS clock. The MAX3674 has excellent period jitter, cycle-to-cycle jitter, and supply noise rejection performance. With output frequencies programmable from 21.25MHz to 1360MHz and support of two differential PECL output signals, the device provides a versatile solution for the most demanding clock applications. Programming is accomplished through a 2-wire I²C bus or parallel interface that can change the output frequency on demand for frequency margining. Both LVPECL outputs have synchronous stop functionality, and the PLL has a LOCK indicator output. The MAX3674 operates from a +3.3V supply and typically consumes 396mW. The device is packaged in a 48-pin LQFP, and the operating temperature range is from -40°C to +85°C.

II. Manufacturing Information

A. Description/Function:	High-Performance, Dual-Output, Network Clock Synthesizer
B. Process:	
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Carsem
F. Date of Initial Production:	December 7, 2007

III. Packaging Information

A. Package Type:	48-pin LQFP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2681
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Multi Layer Theta Ja:	46°C/W
K. Multi Layer Theta Jc:	10°C/W

IV. Die Information

A. Dimensions:	110 X 108 mils
B. Passivation:	Laser/TEOS Ox - Pass/Nit -PreLP+GenLP
C. Interconnect:	Al/Cu 0.5%
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 048 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.4 \times 10^{-9}$

$\lambda = 22.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the TSMC 0.18um Process results in a FIT Rate of 0.8 @ 25C and 13.1 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The HD87 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX3674ECM+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data