



## FAILURE MECHANISMS FOR TRANSIENT VOLTAGE SUPPRESSORS

In most applications, anticipated transient threats are well defined as exemplified in the RTCA DO-160 specification for avionics or in international standards such as IEC-1000-4-2, IEC-1000-4-4, and IEC-1000-4-5 where the open-circuit-transient voltage ( $V_{OC}$ ) and short-circuit current ( $I_{SC}$ ) are identified. From these values, the Peak Pulse Current ( $I_{PP}$ ) and Peak Pulse Power ( $P_{PP}$ ) can be determined as described in MicroNotes 125, 126, and 127 for properly selecting a TVS to ensure adequate surge capabilities. However in some applications, this same needed information for quantifying transients and their source is not well defined due to the obscure overall nature of various possible transient events.

This can also eventually generate other questions in what failure mechanisms exist for silicon p-n junction Transient Voltage Suppressor (TVS) when overstressed. That becomes important since it is located in front of a sensitive load as a parallel shunt path to redirect any high voltage transient threats to ground before they damage the load it is intended to protect. NOTE: When a TVS is properly selected in voltage, it is transparent to the circuit or simply idling at a very low Standby Current ( $I_D$ ) at less than or equal to its rated Reverse Standoff Voltage ( $V_{WM}$ ) until a higher transient voltage occurs that drives the device briefly into its avalanche breakdown region.

The silicon p-n junction TVS device is also identified as an “ABD” or Avalanche Breakdown Diode Transient Voltage Suppressor in IEC or JEDEC standards such as JESD210. When avalanche breakdown occurs, the silicon p-n junction device conducts a large amount of current ( $I_{PP}$ ) to ground in front of the protected load for a short duration transient that is typically 1 ms or less. During this short event, the TVS device clamps the voltage to a safe level ( $V_C$ ). This also results in significant power ( $P_{PP}$ ) and heating at the p-n junction. This can repeat itself for random recurring transient events indefinitely within the rating of the TVS but only if there is sufficient time for the device to cool before the next event occurs. Rapid repetitive surges that would cause cumulative heating effects are not part of the normal rating of a TVS as described in MicroNote 133. Silicon p-n junction TVS devices are unlike Metal Oxide Varistor (MOV) devices that can degrade over time after many random recurring surges within their maximum rating.

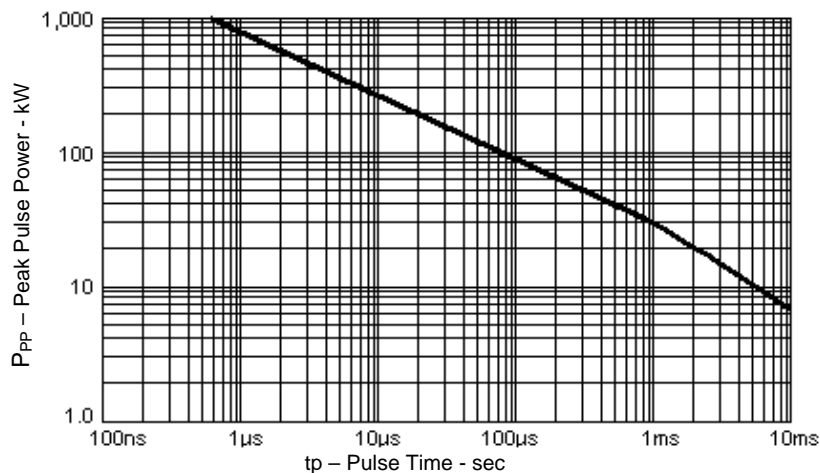
When individual excessive surges occur beyond the rating of the TVS, these devices can fail just like any other semiconductor component when exceeding their ratings. For TVSs, this primarily involves excessive Peak Pulse Power ( $P_{PP}$ ) and/or Peak Pulse Current ( $I_{PP}$ ). The basic form of failure mechanism is attributable to excessive heat in the active p-n junction of the silicon element. This is also dependent on the pulse width of the transient threat where  $P_{PP}$  capabilities for a TVS decline in a predictable manner with longer pulse widths as described in MicroNotes 104 and 120. The capabilities in  $P_{PP}$  generally follow what has historically been recognized as a Wunsch-Bell Curve.



## EXCEEDING TVS PEAK PULSE POWER ( $P_{PP}$ ) RATINGS

The  $P_{PP}$  versus pulse time performance curve found in Figure 1 of most of the Microsemi data sheets is a straight line with a negative slope on a log-log plot. It is typically shown for short transients up to 1 ms (sometimes longer) for most device types. The negative slope in these figures declines one decade in  $P_{PP}$  for every two decades in increasing pulse width indicating in mathematical terms the  $P_{PP}$  is inversely proportional to the square root of pulse width.

This relationship for rating a TVS and its maximum  $P_{PP}$  capabilities correlate to a relatively constant elevated p-n junction temperature before failure regardless of pulse duration time. These p-n junction temperatures can briefly approach  $275^{\circ}\text{C}$  during the surge without damaging the device. The example shown below in Figure 1 is for a 30 kW rated TVS device at 1 ms and  $25^{\circ}\text{C}$ . For higher device or ambient temperatures, the  $P_{PP}$  capabilities are derated as also shown in most TVS data sheets as also described in MicroNotes 114 and 115.



**FIGURE 1**  
Peak Pulse Power vs. Pulse Time

This same characteristic behavior is also shown for other Microsemi TVS product data sheets where devices with lower  $P_{PP}$  ratings will portray the same negative slope except be positioned lower with respect to the ordinate ( $P_{PP}$ ) axis. The intersection at 1 ms will coincide with its  $P_{PP}$  rating at  $25^{\circ}\text{C}$  if referenced at  $10/1000 \mu\text{s}$ . This is the industry method of identifying a double exponential impulse with a  $10 \mu\text{s}$  rise time to the peak and a  $1000 \mu\text{s}$  to the 50 % decay point.



## TVS FAILURE MECHANISMS

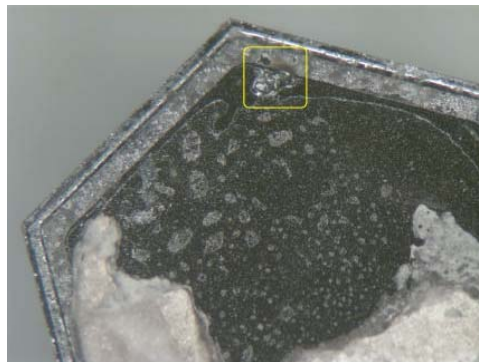
With that background, we can better describe specific failure mechanisms when TVSs are pushed above their  $P_{PP}$  ratings where p-n junction temperatures start exceeding a safe operating level during a surge event. The extent that a surge exceeds specified  $P_{PP}$  ratings may also dictate failure mode and its severity.

### HOT SPOTS AND ELECTRICAL SHORTS

In the vast majority of cases, a TVS will fail in a shorted or severely degraded mode when overstressed. For many applications, that has often been the preferred failure mode since the device would then protect the remaining sensitive circuit from further severe transient threats due to its “electrically shorted” shunt path to ground in front of the protected load until the device is replaced.

As p-n junction temperatures quickly increase during a transient beyond device ratings, it eventually forces the device into its “intrinsic” region where it no longer operates as a semiconductor and instead becomes a resistor. This occurs when the concentration of thermally generated electron-hole pairs at high temperatures approach or exceeds the background p or n doping levels of a TVS device thus compromising the semiconductor characteristic features of the p-n junction. This will initially occur in higher voltage TVS devices that have a lower concentration in background doping level for higher avalanche breakdown voltages as dictated by the overall semiconductor physics in diode device designs. When that happens at very high p-n junction temperatures, the TVS device voltage characteristics start to collapse due to excessive leakage currents during the transient event and thermal runaway will quickly occur. This collapse in voltage features of the TVS may also include the possibility of high “follow-on currents” through the device depending on the operating voltage and load-line features of the circuit it is in.

This rapid failure mode typically creates a “hot spot” somewhere in the p-n junction as well as permanent damage up to and including a localized silicon melt region from front to back of the active die element. That feature becomes very destructive as becomes very evident in a physical analysis shown below in Figure 2.



**Figure 2 Hot Spot Failure Mode**

This described localized-melt region is an alloy formation of silicon combined with adjoining ohmic-contact metallization or solder materials resulting in a highly conductive “pipe” region from front to back of the silicon die. It may also result in micro cracks from thermal stresses propagating outward from the hot-spot region. Although these secondary cracks in the active silicon die will also increase leakage current and voltage degradation, the major failure mechanism is the hot spot itself.

This very rapid catastrophic event during a transient Electrical Over Stress (EOS) also explains why there are very few (if any) occurrences of only slight degradation due to a surge overstress. It has either failed in a significant manner due to thermal runaway or it is still good. The described mode of degradation (if not shorted) is where the TVS silicon internal element only supports a minimal value in voltage with very high leakage currents and minimal resistance such as a few Ohms or less.

In other application scenarios where an excessive amount of dc voltage or current (power) is applied, the device will be driven into continuous breakdown similar to a Zener. If that dc power is excessive, it will also eventually overheat if it is not fused open by design on the line being protected by the TVS. During this period of time the breakdown voltage will again rise due to the positive temperature coefficient of avalanche breakdown for  $V_Z$  or  $V_{BR}$  as would a Zener (see Micronote 203). Some of these scenarios of operating a TVS as a Zener or vice-versa is also discussed in MicroNote 134. The amount of heating (and voltage rise) with continuous applied power is also dependent on heat sinking provided to the device. The maximum voltage may briefly approach the maximum clamping voltage ( $V_C$ ) from similar high p-n junction temperatures as earlier noted during surge. This is primarily due to the positive temperature coefficient of avalanche breakdown. Before device failure, it still can serve as a shunt regulator protecting a load from excessive voltages. However this type of sustained heating is not desirable and can eventually reflow internal solders (if applicable) closest to the p-n junction where notable energy (heat) is generated with applied power and time. This can also eventually result in a short circuit path generated by solder reflow either around the p-n junction or through it if localized hot spots are again generated by excessive heat within the die element."

## LOSS OF CONTACT AND ELECTRICAL OPENS

In most applications, the loss of contact or electrical opens is not a desirable EOS failure mode for a TVS in its shunt protective position in the circuit since that would expose the remaining sensitive load to subsequent transient threats. An electrical open of the TVS location can also make it difficult to verify anything is wrong until a subsequent surge occurs that may damage the remaining circuit requiring protection. Nevertheless for some severe forms of EOS, that failure mode can occur with TVS devices. In those unusual circumstances, the following is provided to further describe the possible failure modes and how to minimize their occurrence if that type of failure mode is not desired.



## AVOIDING ELECTRICAL OPENS

In applications where an electrical open failure is to be avoided at the TVS location in the circuit, precautions are appropriate in how package termination(s) are attached or heat sunk. This avoids risk of them either being broken or melted off from a sustained heat soak that can follow a surge event or sustained power overload. A further extended heat soak can occur if a TVS failure does not become a dead short and must still dissipate significant sustained power with very high follow-on currents. This is particularly a concern if there is minimal source resistance in the circuit (such as a power buss). For these reasons, a fuse can also be placed in the circuit to prevent overheating of PCB traces or of a severely degraded TVS component that may still be dissipating power in a low resistive state without completely shorting electrically.

TVS designs using a double-plug glass body configuration can break mechanically in half when severely overstressed resulting in an electrical open. The probability of this type failure mechanism increases as severity of transient power also increases well beyond the device ratings. When the die is quickly heated to extremes in such examples by a severe transient, there is no internal strain relief mechanism when the entrapped die also expands very rapidly between two plugs surrounded by a glass body. In those cases, it ultimately breaks the glass body into two parts at the location of the active die element. To avoid these type failures, conservative selection in  $P_{pp}$  for TVSs beyond the expected threat level requirements will minimize these catastrophic failure modes. This includes consideration for  $P_{pp}$  temperature derating as described in MicroNotes 114 and 115.

In small size TVS array designs involving internal wire bonds that are only intended for very short transients of 8/20  $\mu$ s or less such as ESD protection, there are other failure modes possible when significantly exceeding  $P_{pp}$  ratings for these smaller devices. The internal wire bond designs used in these smaller designs between the die and package lead frame can fuse open. Small individual internal wire bonds are not used on higher  $P_{pp}$  rated TVSs for these reasons where instead large lead or lead-frame contacts are bonded directly to the active TVS element. For those hybrid applications requiring the use of larger TVS die or chips, it is recommended that the use of multiple wire bonds be made. Also the use of a metal disc bonded to the top side of the die should be used before wire bonding to the disc. This serves as a “current-spreader” across the face of the die (rather than allow high surge current concentrations to occur under a wire bond). The disc can also serve as a heat sink for a short transient to make for a more efficient application of the active die size used.

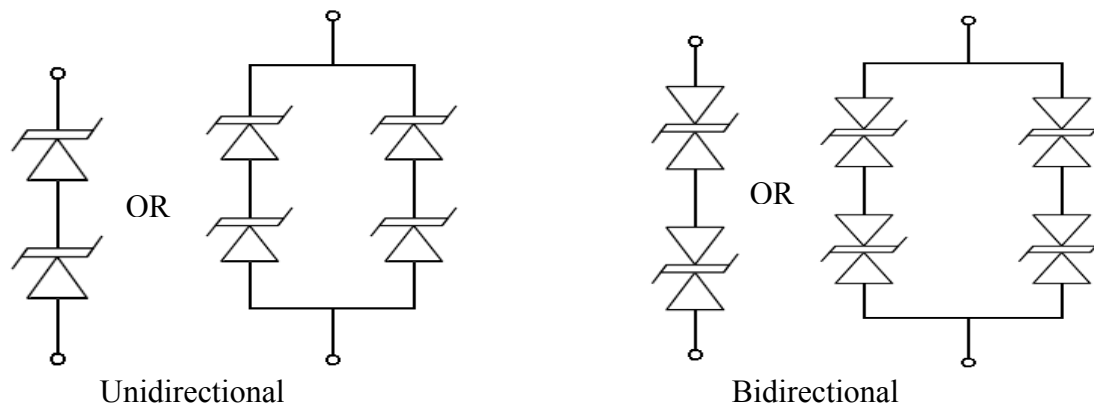
Despite design precautions in protecting from various known transient threats, some transients can also be allusive by their very nature. For example there can be extreme transients with sufficient energy such as very close proximity lightning strikes or nearby severe inductive load switching to literally cause the TVS device to vaporize at their weakest points from extreme  $P_{pp}$  energy levels causing an electrical open. These type events are rare compared to the other failure mechanisms described in this MicroNote.



## CONSERVATIVE TVS DESIGN OPTIONS

In very conservative design applications such as satellites where any failure becomes critical, redundant circuits are often used. Using that same principle, TVSs may be applied in such a manner where any single component failure will not significantly affect the application. For example, two TVS devices may be placed in series in those areas where twice the Clamping Voltage ( $V_C$ ) of any one TVS device is still adequate to protect the sensitive load behind the TVS and the Working Standoff Voltage ( $V_{WM}$ ) of one device is still sufficient for normal operation. If any one TVS device in series becomes electrically shorted or severely degraded, the remaining device in series still provides protection. As described earlier, a TVS device is simply idling at very low leakage current in its normal operating mode at  $V_{WM}$  until a high voltage transient drives it into avalanche breakdown. Higher voltage selections of  $V_{WM}$  will not be an issue unless the  $V_C$  is excessive for the needed sensitive load protection. This includes the effects resulting from two TVS devices in series. However in many applications, the sensitive load being protected does not allow much voltage overhead. More on that subject is discussed in MicroNote 134.

In those cases where an unusual electrical open of any one TVS device may be of concern, then two such legs of TVSs are provided in parallel representing a total of four (4) TVS devices. Such configurations for TVSs also increase the  $P_{PP}$  capabilities for conservative design as described in MicroNotes 112 and 113. These conservative application methods can also be used with unidirectional or bidirectional TVS devices as shown below in Figure 3.



**Figure 3**  
**Conservative TVS Circuit Designs**

In summary, the primary failure mode of TVSs is a severely degraded device that has collapsed in voltage or become an electrical short. Nevertheless there can be other failure modes depending on the severity of electrical overstress. Using conservative approaches by selecting TVSs with generous  $P_{PP}$  ratings helps diminish these other less desirable failure modes.



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